»Kontron User's Guide«

AdvancedMC™

AM4211

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Revision History

Rev. Index	Brief Description of Changes	Date of Issue
1.0	First Release	May 2012

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Safety Instructions

Before You Begin

Before handling the board, read the instructions and safety guidelines on the following pages to prevent damage to the product and to ensure your own personal safety. Refer to the "Advisory Convention" section in the Preface for advisory conventions used in this user's guide, including the distinction between Warnings, Cautions, Important Notes, and Notes.

- Always use caution when handling/operating the computer. Only qualified, experienced and authorized electronics service personnel should access the interior of the computer. The power supplies produce high voltages and energy hazards, which can cause bodily harm.
- Use extreme caution when installing or removing components. Refer to the installation instructions in this user's guide for precautions and procedures. If you have any questions, please contact Kontron Technical Support.

WARNING

High voltages are present inside the chassis when the unit's power cord is plugged into an electrical outlet. Turn off system power, turn off the power supply, and then disconnect the power cord from its source before removing the chassis cover. Turning off the system power switch does not remove power to components.

Preventing Electrostatic Discharge

Static electricity can harm system boards. Perform service at an ESD workstation and follow proper ESD procedure to reduce the risk of damage to components. Kontron strongly encourages you to follow proper ESD procedure, which can include wrist straps and smocks, when servicing equipment.

Take the following steps to prevent damage from electrostatic discharge (ESD):

- When unpacking a static-sensitive component from its shipping carton, do not remove the component's antistatic packing material until you are ready to install the component in a computer. Just before unwrapping the antistatic packaging, be sure you are at an ESD workstation or grounded. This will discharge any static electricity that may have built up in your body.
- When transporting a sensitive component, first place it in an antistatic container or packaging.
- Handle all sensitive components at an ESD workstation. If possible, use antistatic floor pads and workbench pads.
- Handle components and boards with care. Don't touch the components or contacts on a board. Hold a board by its edges.
- Do not handle or store system boards near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Safety Requirements

The following safety precautions must be observed when installing or operating the AM4211. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

WARNING

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.
In addition, the board should not be placed on any surface or in any form of storage container until the board and heat sink have cooled down. Remove the such time as have cooled down to room temperature.

ESD Equipment

This AMC board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

WARNING

This product has gold conductive fingers which are susceptible to contamination. Take care not to touch the gold conductive fingers of the AMC Card-edge connector when handling the board.
Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

CAUTION

Laser light from fiber-optic transmission cables and components can damage your eyes. The laser components plugged into the switch are Class 1 laser components. Class 1 laser is considered incapable of producing damaging radiation levels during normal operation or maintenance.
To avoid damaging your eyes and to continue safe operation in case of abnormal circumstances:

- Never look directly into the outlets of fiber-optic transmission components or fiber-optic cables with unprotected eyes.
- Never allow fiber-optic transmission path to operate until all the connections have been made.

Always fit protective plugs to any unused ports of the switch.

WARNING

Be careful when inserting or removing the AM4211. The SFP+ cage has sharp edges which might lead to injuries.

Preface

How to Use This Guide

This user's guide is designed to be used as step-by-step instructions for installation, and as a reference for operation, troubleshooting and upgrades.

For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

The following is a summary of chapter contents:

- Chapter 1, Product Description
- Chapter 2, Board Features
- Chapter 3, Installing the board
- Chapter 4, Thermal
- Chapter 5, Software Setup
- Appendix A, Connector Pinouts
- Appendix B, Getting Help
- Appendix C, Glossary

Customer Comments

If you have any difficulties using this user's guide, discover an error, or just want to provide some feedback, please send a message to: Tech.Writer@ca.kontron.com. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user's guide on our Web site. Thank you.

Advisory Conventions

Seven types of advisories are used throughout the user guides to provide helpful information or to alert you to the potential for hardware damage or personal injury. They are Note, Signal Paths, Jumpers Settings, BIOS Settings, Software Usage, Cautions, and Warnings. The following is an example of each type of advisory. Use caution when servicing electrical components.

Note:
Indicates information that is important for you to know.

Signal Path:
Indicates the places where you can find the signal on the board.

Jumper Settings:
Indicate the jumpers that are related to this section.

BIOS Settings:
Indicates where you can set this option in the BIOS.

Software Usage:
Indicates how you can access this feature through software.

CAUTION
Indicates potential damage to hardware and tells you how to avoid the problem.

WARNING
Indicates potential for bodily harm and tells you how to avoid the problem.

ESD Sensitive Device:
This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.
Please read also the section "Special Handling and Unpacking Instructions".

CE Conformity:
This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section "Regulatory Compliance Statements" in this manual.

Disclaimer: We have tried to identify all situations that may pose a warning or a caution condition in this user's guide. However, Kontron does not claim to have covered all situations that might require the use of a Caution or a Warning.

Unpacking

Follow these recommendations while unpacking:

- Remove all items from the box. If any items listed on the purchase order are missing, notify Kontron customer service immediately.
- Inspect the product for damage. If there is damage, notify Kontron customer service immediately.
- Save the box and packing material for possible future shipment.

Regulatory Compliance Statements

FCC Compliance Statement for Class B Devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generated, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experience radio/TV technician for help.

WARNING

This is a Class B product. If not installed in a properly shielded enclosure and used in accordance with this User's Guide, this product may cause radio interference in which case users may need to take additional measures at their own expense.

Safety Certification

All Kontron equipment meets or exceeds safety requirements based on the IEC/EN/UL/CSA 60950-1 family of standards entitled, "Safety of information technology equipment. " All components are chosen to reduce fire hazards and provide insulation and protection where necessary. Testing and reports when required, are performed under the international IECEE CB Scheme. Please consult the "Kontron Safety Conformity Policy Guide" for more information.

CE Certification

The product(s) described in this user's guide complies with all applicable European Union (CE) directives if it has a CE marking. For computer systems to remain CE compliant, only CE-compliant parts may be used. Maintaining CE compliance also requires proper cables and cabling techniques. Although Kontron offers accessories, the customer must ensure that these products are installed with proper shielding to maintain CE compliance. Kontron does not offer engineering services for designing cabling systems. In addition, Kontron will not retest or recertify systems or components that have been reconfigured by customers.

Limited Warranty

Kontron grants the original purchaser of Kontron's products a TWO YEAR LIMITED HARDWARE WARRANTY as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron.

Kontron warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long- term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than Kontron or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation.

Kontron provides for repair or replacement of any part, assembly or sub-assembly at their own discretion, or to refund the original cost of purchase, if appropriate. In the event of repair, refunding or replacement of any part, the ownership of the removed or replaced parts reverts to Kontron, and the remaining part of the original guarantee, or any new guarantee to cover the repaired or replaced items, will be transferred to cover the new or repaired items. Any extensions to the original guarantee are considered gestures of goodwill, and will be defined in the "Repair Report" issued by Kontron with the repaired or replaced item.

Kontron will not accept liability for any further claims resulting directly or indirectly from any warranty claim, other than the above specified repair, replacement or refunding. In particular, all claims for damage to any system or process in which the product was employed, or any loss incurred as a result of the product not functioning at any given time, are excluded. The extent of Kontron liability to the customer shall not exceed the original purchase price of the item for which the claim exists.

Kontron issues no warranty or representation, either explicit or implicit, with respect to its products reliability, fitness, quality, marketability or ability to fulfil any particular application or purpose. As a result, the products are sold "as is," and the responsibility to ensure their suitability for any given task remains that of the purchaser. In no event will Kontron be liable for direct, indirect or consequential damages resulting from the use of our hardware or software products, or documentation, even if Kontron were advised of the possibility of such claims prior to the purchase of the product or during any period since the date of its purchase.

Please remember that no Kontron employee, dealer or agent is authorized to make any modification or addition to the above specified terms, either verbally or in any other form, written or electronically transmitted, without the company's consent.

Chapter 1

Product Description

1. Product Description

1.1 Product Overview

The AM4211 is an Advanced Mezzanine Card (AMC) from Kontron supporting the Cavium OCTEON II CN6645 Network Service Processor. It is cost and performance competitive with other NSP AdvancedMC cards featuring similar number of cores and process technology. The big advantage of the Cavium NSP is it's broad market acceptance and large ecosystem solution providers. It is also an excellent choice for future upgrade to the existing Cavium OCTEON Plus AM42xx series offered by Kontron.

The AM4211 is a 10 GbE card with one 10 Gb Ethernet port on front panel using a SFP+ cage and software configurable Interfaces to the Fabric side (one PCIe/SRIO on ports 4 to 7 and one PCIe/SGMII/XAUI on ports 8 to 11).

Two Gigabit Ethernet Ports are connected to ports 0 and 1 of the AMC connector.

A debug port is accessible via a low profile serial port connector on front plate or AMC port 15 of Extended Option Region. Two different UART can be routed at the same time in two differents places (ex: CPU UART0 to front, CPU UART1 to rear).

An eUSB mezzanine that has a capacity of up 16 GB is available for storage.

1.2 What's Included

This board is shipped with the following items:

- One AM4211 AMC board;
- One Quick Reference Sheet;
- One low profile serial port to D-sub (female) adapter cable (1016-6698);
- One Documentation & Drivers disk;

If any item is missing or damaged, contact your supplier.

1.3 Board Specifications

Table 1-1: Board Specifications

Features	Description
Multicore Processor Unit	• CN6645 Cavium OCTEON II processor capable of supporting 10 Cores at 1.1 GHz • Socketless
Memory	• 1 to 32 GB DDR3 Memory support with ECC • Up to 1333 MHz ECC SO-DIMM
Flash Memory	• 128MB NOR Flash • Boot sector protection
eUSB Storage	• Single Port USB 2.0 interface
Dual Gigabit Ethernet Controller	• Dual Gigabit Ethernet Controller Broadcom BCM5482 • SGMII interface to processor • 2 1000Base-BX (Serdes) interfaces to AMC connector
IPMI	• IPMI 2.0 compliant • Voltage and Temperature Sensors • ATCA LED control • FRU data storage for AMC • Firmware Update handling for field upgrades, rollbacks and watchdog functions
I/O Interfaces	• Front: 1 SFP+ cage to support multi-rate fiber SFP+ modules • Front: low profile connector for RS232 access to Processor • AMC TCLKA and TCLKC support • AMC FCLKA input with 100MHz • AMC Port 0 and Port 1: 1000Base-BX • AMC port 4 to 7 : Configurable PCIe Gen 2 5 GT/s x4 or SRIO x4 Level I (up to 3.125 GBaud) • AMC port 8 to 11: PCIe Gen2 5GT/s x4, XAUI or SGMII • AMC Port 15: RS232 (proprietary mapping)

Features	Description
Standards Compliance	This board is compliant to the following standards: • AMC.0 R2.0 Advance Mezzanine Card Base Specification • AMC.1 R2.0 PCI Express and Advance Switching • AMC.2 R1.0 Ethernet Specification • AMC.4 R1.0 Serial RapidIO Specification • MTCA.0 R1.0 Micro Telecommunication Computing Architecture Base Specification • IPMI v2.0. • RoHS compliant.
Mechanical Characteristics	• 4HP single Mid-size AMC Module
Operating Voltages	• Management: 3.3V +/-0.3V • Payload: 10VDC to 14VDC
Operation Power	• Management: 0.495 W max., TBD W typ. • Payload: 40 W max., TBD W typ.
Temperature	• Operates from -5°C to 55°C ambient air temperature with forced convection. Based on B.4. chassis. • Operating @ 8 CFM: up to 25°C • Operating @ 11.4 CFM: 26°C to 40°C • Operating @ 18.0 CFM: 41°C to 55°C • Non-Operating: -40°C to 85°C
Humidity	• Designed to meet Bellcore GR-63, Section 4.1 • Operating: 5%-93% (non-condensing) at 40°C • Non-Operating: 5%-93% (non-condensing) at 40°C
Altitude	• Designed to meet the following requirements according to Belcore GR-63, section 4.1.3: • Operating: -300 m to 4,000 m (13123 ft) (GR63 4.1.3), may require additional cooling above 1800m (5905ft) • Non-Operating: -300 m to 14,000 m (45931.2 ft)
Shock & Vibration	• Designed to meet EN 300 019 and Telcore GR-63 • Designed to meet NEBS Level 3, Earthquake Zone 4
Safety	• Low Voltage Directive 2006/95/EC • Complies with IEC/EN/CSA/ UL 60950-1 • The board meets flammability requirement, as specified in Telcordia GR-63 • UL 94V-0/1 with Oxygen index of 28% or greater material
Electromagnetic Compatibility	• Meets or exceeds the following specifications (assuming an adequate chassis): • EMC Directive 2004/108/EC • EN55022; EN55024; CISPR22; VCCI • EN 300 386 • FCC 47 CFR Part 15 • Telcordia GR-1089

1.4 Hot Swap Capability

The AMC supports Full Hot Swap capability as required by AMC.0 R2.0. It can be removed from or installed in the system while it is on (without powering-down the system). Please refer to the AMC.0 R2.0 specification for additional details.

1.5 Software Support

The following table contains information related to software supported by the AM4211.

Table 1-2: AM4211 Software Specification

	Specifications
General	• The system supports IPMI version 2.0 for board level management (AMC.0). • Support for onboard IPMI event log (SEL) • Reliable field upgrades for all software components, including boot loader and IPMI firmware • Optional Dual boot images with roll-back capability. • Offline Diagnostic software for running diagnostic tests
Bootloader	U-Boot • Power On Self Test • Loadable boot image from onboard flash • Reliable field upgradable • KCS interface to MMC • Serial console support
Operating System	Linux Operating System is based on Cavium SDK 2.2.0 (2.6.32).

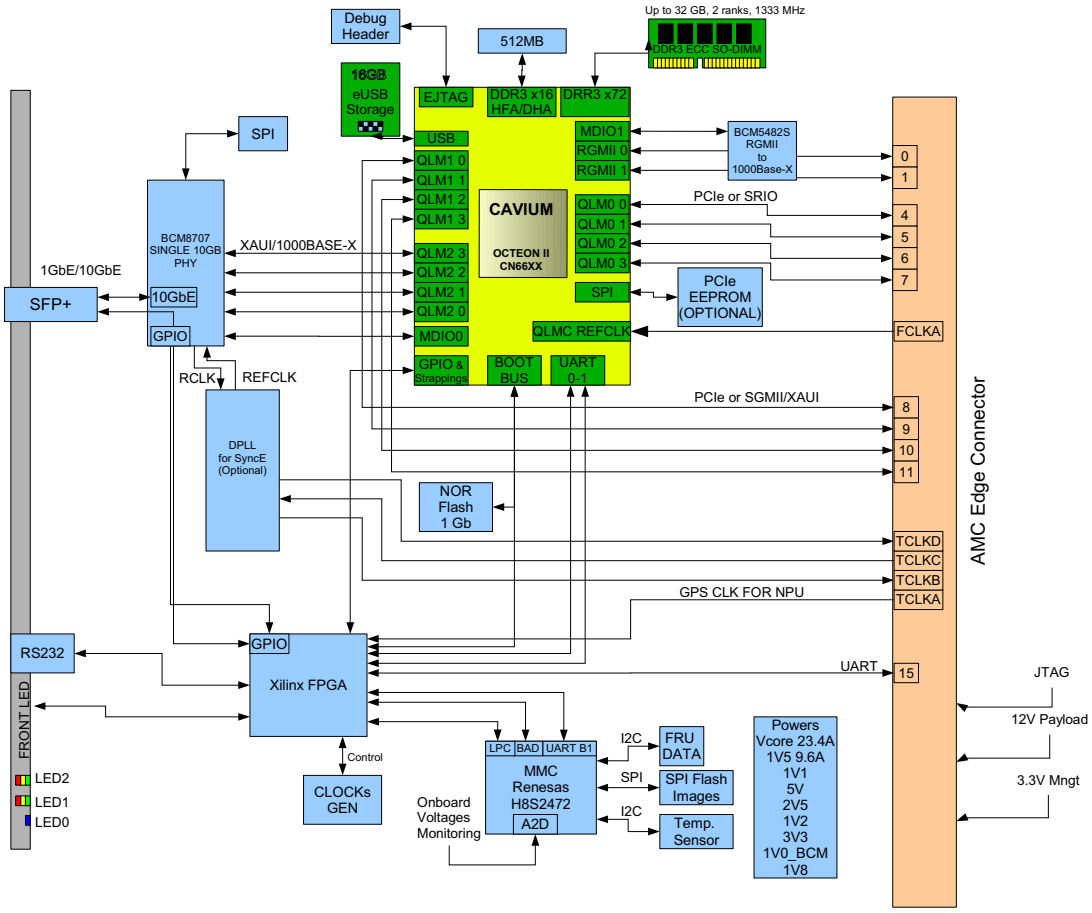
Chapter 2

Board Features

2. Board Features

2.1 Block Diagram

Figure 2-1:Block Diagram



2.2 System Core

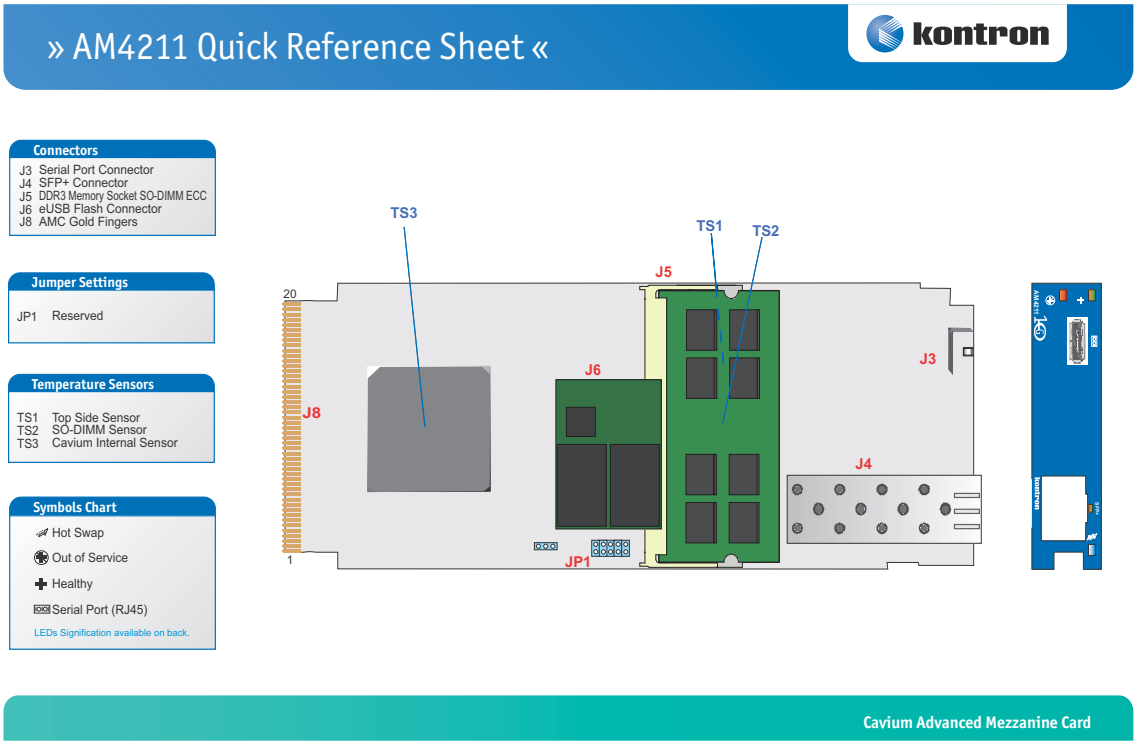
2.2.1 Cavium OCTEON II CN6645

- Ten(10) Cores at 1.1GHz
- Up to 30 Billion MIPS64 instructions per second
- 12 high-speed SERDES, flexibly configured in blocks of 4 (referred to as QLM)
- XAUI, SGMII, PCIe or SRIO depending on QLM
- Integrated coprocessors for application acceleration, including: Packet I/O processing, QoS, TCP Acceleration; Support for IPsec, SSL, SRTP, WLAN and 3G/UMB/LTE security (includes DES, 3DES, AES-GCM, AES up to 256, SHA1, SHA-2 up to SHA-512, RSA up to 8192, DH, KASUMI); and Compression/ Decompression with up to 10Gbps throughput and highest compression ratios.

2.3 eUSB Storage

The AM4211 supports one (1) Solid State Drive. It is a NAND flash disk module with a USB 2.0 interface. The module is connected to a 2x5 header (refers to J6 on showed in Figure 2-2) on the AM4211 board.

Figure 2-2:AM4211 Quick Reference Sheet



Signal Path:

USB Flash Module Connector is located close to the heatsink and the memory socket.

2.4 SFP+ Front IO

The front SFP+ cage supports a multi-rate fiber SFP+ module.

Table 2-1: SFP+ Connection

SFP+	Connection
1	10 GbE XAUI

SFP+ module is not provided with the AM4211 and has to be obtained separately. The SFP+ uplink port is compliant to the Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module “SFP+” MultiSource Agreement (MSA), February 16th 2007, and the Improved Pluggable Formfactor MSA, February 26th 2007. An application note with a list of SFP+ modules successfully operated by Kontron in the AM4211 is available upon request.

CAUTION LASER LIGHT!

Do not look into the laser beam!
The SFP+ module is fitted with a class 1 or 1M laser. To avoid possible exposure to hazardous levels of invisible laser radiation, do not exceed maximum ratings.

The SFP+ port has a bi-color green/amber LED with the following signification:

Table 2-2: SFP+ LED Significations

LED	Signification
Green on	Link 10Gbit
Green blink	Activity 10Gbit
Amber on	Link 1000Mbit

2.5 Gigabit Ethernet

Two Gigabit Ethernet Ports are connected to ports 0 and 1 of the AMC connector.

Signal Path:

Two Gigabit Ethernet Ports are connected to ports 0 and 1 of the AMC connector.

2.6 Serial Rapid I/O (SRIO)

AMC provides SRIO x4 interfaces only as per AMC.4 R1.0 fat pipe region on ports 4 to 7. The supported SRIO speed are using a priority order controlled by E-Keying mechanism.

SRIO speed priority list:

SRIO 3.125Gbs

SRIO 2.5Gbs

SRIO 1.25Gbs

Signal Path:
Serial Rapid I/O is connected to ports 4 to 7 of the AMC connector.

2.7 PCIe

AMC provides two independant PCIe links. A PCIe x4 Gen2 interface on fat pipe region ports 4 to 7 as per AMC.1 R2.0. And a PCIe x4 Gen2 interface on the extended fat pipe region ports 8 to 11.The supported PCIe modes are using a priority order controlled by E-Keying mechanism.

PCIe mode priority list:

PCIe Gen2 x4 SCC

PCIe Gen2 x4 NoSCC

PCIe Gen2 x1 SCC

PCIe Gen2 x1 NoSCC

PCIe Gen1 x4 SCC

PCIe Gen1 x4 NoSCC

PCIe Gen1 x1 SCC

PCIe Gen1 x1 NoSCC.

Signal Path:
PCIe is connected to ports 4 to 7 and 8 to 11 of the AMC connector.

2.8 SGMII / XAUI

One SGMII / XAUI interface, as per AMC.2 R1.0, is available on ports 8 to 11 in the fat pipes region.

Signal Path:
The SGMII / XAUI is connected to ports 8 to 11 of the AMC connector.

2.9 RS232 Management Interface

The RS232 interface of the OCTEON is connected to the front panel low profile connector.

Use a special cable with low profile serial port connector to SubD connector.

Signal Path:
The serial port is available through the AMC faceplate.

2.10 IPMI

The AM4211 supports an intelligent hardware management system based on the Intelligent Platform Management Interface (IPMI) Specification 2.0. It provides the ability to manage the power, cooling and interconnect needs of intelligent devices, to monitor events and to log events to a central repository.

The MMC (“Module Management Controller”) controls all hotswap and E-Keying processes required by ATCA. It activates the board power supply and enables communication with the AMC carrier. The MMC manages the Ethernet switch E-Keying and the baseboard ATCA feature. The controller is connected to the IPMC of the ATCA carrier board via IPMB-L bus.

All voltages and currents on the board are monitored by the MMC. Three temperature sensors on the board make sure that thermal conditions are met:

- Temp NPU (OCTEON Internal Sensor)
- Temp MMC
- Temp DIMM

For more information on the thermal design and management, consult the “Thermal Consideration” section.

2.11 AMC Connector

Table 2-3: AMC Port Assignment

Port	Region	Connection
0	GbE	GbE eth0
1	GbE	GbE eth1
2	Storage	-
3	Storage	-
4	Fat Pipe	PCIe / SRIO Port 0 (Lane 0)
5	Fat Pipe	PCIe / SRIO Port 0 (Lane 1)
6	Fat Pipe	PCIe / SRIO Port 0 (Lane 2)
7	Fat Pipe	PCIe / SRIO Port 0 (Lane 3)
8	Fat Pipe	PCIe / XAUI / SGMII Port 1 (Lane 0)
9	Fat Pipe	PCIe / XAUI / SGMII Port 1 (Lane 1)
10	Fat Pipe	PCIe / XAUI / SGMII Port 1 (Lane 2)
11	Fat Pipe	PCIe / XAUI / SGMII Port 1 (Lane 3)
12	Extended	-
13	Extended	-
14	Extended	-
15	Extended	RS232
17	Extended	-
18	Extended	-
19	Extended	-
20	Extended	-
TCLKA	Clock	For GPS clock from AMC Connector
TCLKB	Clock	Optional SyncE to the AMC Connector
TCLKC	Clock	Optional SyncE from AMC Connector
TCLKD	Clock	Optional SyncE to the AMC Connector
FCLKA	Clock	PCIe Reference Clock (FCLKA input may be damaged if driven by an M-LVDS driver.)

2.12 Front Panel LEDs

Figure 2-3:Front Panel of AM4211

2.12.1 Hot Swap LED (Blue LED)

The AM4211 board supports a blue Hot Swap LED mounted on the front panel. This LED indicates when it is safe to remove the Module. The on-board MMC drives this LED to indicate the hot swap state but is controlled by the carrier's IPMC or the MicroTCA carrier manager. The following states are possible:

Table 2-4: Hot Swap LED

LED state	Description
OFF	Module is in M3 or M4 state, normal state when module is in operation.
ON	Module is ready for hot swap
Short blink	Module is in M5 state (Deactivation Request) or in M6 state (Deactivation in progress)
Long blink	Activation in progress.

2.12.2 Out-Of-Service (OOS) LED (LED1)

Table 2-5: Red LED

LED state	Description
ON	MMC in reset
Blinking	MMC upgrade / rollback in progress
OFF	MMC operational
Application Defined	May be controlled by application using PICMG API

2.12.3 Health LED (LED2)

Table 2-6: Amber/Green LED

LED state	Description
OFF	Payload power down
Green	Payload is On and no critical event is detected by the sensors
Amber	Payload is On and at least one critical event is detected by the sensors
Application Defined	May be controlled by application using PICMG API

2.12.4 SFP + LED

Table 2-7: Amber/Green LED

LED state	Description
Green OFF	no 10GbE link
Green ON	10GbE link
Green Blink	10GbE traffic
Amber OFF	no 1000Base-x link
Amber ON	1000Base-x link

Chapter 3

Installing the Board

3. Installing the Board

3.1 Hot Swap Insertion Procedures

The AM4211 is designed for hot swap operation. Hot swapping allows the coordinated insertion and extraction of modules without disrupting other operational elements within the system. This allows for identified faulty elements to be removed and replaced without taking the carrier card out of service that will typically be hosting others modules.

The following procedures are applicable when inserting the AM4211 in a running system.

1 Ensure that the safety requirements are observed.

WARNING

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2 Ensure that the board is properly configured for operation in accordance with application requirements before installing.

WARNING

Care must be taken when applying the procedures below to ensure that neither the AM4211 nor other system boards are physically damaged by the application of these procedures.

3 To install the AM4211, perform the following:

1 Carefully insert the board into the slot designated by the application requirements until it makes contact with the AMC Card-edge connector located on the carrier or backplane.

2 Connect all external interfacing cables to the board as required.

3 Using the handle on the front panel, engage the board with the carrier or backplane. When the handle is locked, the board is engaged and the following steps occur:

1 The BLUE HS LED turns on.

If the carrier recognizes that the AM4211 is fully seated, the carrier then enables the management power for the AM4211 and the BLUE HS LED turns on.

2 Long blinks of the BLUE HS LED.

If the carrier IPMI controller detects the AM4211, it sends a command to the AM4211 to perform long blinks of the BLUE HS LED.

3 The BLUE HS LED turns off.

The Intelligent Platform Management Controller on the carrier reads the Module Current Requirements record and the AMC Point-to-Point Connectivity record. If the Module FRU information is valid and the carrier can provide the necessary payload power, the BLUE HS

LED will be turned off. If the module FRU information is invalid or the carrier cannot provide the necessary payload power, the insertion process is stopped and the BLUE HS LED keeps blinking. Should this problem occur, please contact Kontron's Technical Support.

4 Short blinks of the Module Management LEDs and the User-Specific LEDs.

The carrier enables the payload power for the AM4211, and the Module Management LEDs and the User-Specific LEDs emit a short blink.

5 Ensure that the board and all required interfacing cables are properly secured.

4 The AM4211 is now ready for operation. Refer to appropriate AM4211- specific software, application, and system documentation for operating instructions, etc.

3.2 Hot Swap Extraction Procedures

To extract the board, proceed as follows:

1 Ensure that the safety requirements, listed at page ix above, are observed. Particular attention must be paid to the warning regarding the heat sink!

2 Pull the handle on the AM4211's front panel initiating the deactivation. This changes the state of the handle to open. Now, the following steps occur:

1 Short blinks of the BLUE HS LED

- When the carrier IPMI controller receives the handle opened event, the carrier sends a command to the MMC with a request to perform short blinks of the BLUE HS LED. This indicates to the operator that the AM4211 is waiting to be deactivated.
- Now the AM4211 waits for a permission from higher level management (Shelf Manager or System Manager) to proceed with its deactivation.
- Once the AM4211 receives the permission to continue the deactivation, all used ports are disabled.
- The Intelligent Platform Management Controller on the Carrier disables the AM4211's Payload Power.

2 The BLUE HS LED turns on.

- Now the AM4211 is ready to be safely extracted.

3 Disconnect any interfacing cables that may be connected to the AM4211.

4 Pull the AM4211 out of the slot. Now the carrier disables the management power for the AM4211.

WARNING

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when handling the board.

3.3 Memory

The AM4211 has one memory channel connected to the Octeon processor. There is one SO-DIMM populated in an SO-DIMM socket. The AM4211 accepts DDR3, SO-DIMM, registered or unregistered, ECC, x8 or x16, with up to 2 ranks. The DDR3 channel supports data rates up to 1333Mhz. The maximum memory that the board will accept is 32GB, although 8GB is the highest capacity tested to date.

Only use validated memory with this product. Thermal issues or other problems may arise if non-recommended modules are used. At the time of publication of this user guide, the following memories have been qualified and approved. As the memory market is volatile, this list is subject to change, please consult your local technical support for an up to date list.

3.3.1 Memory List and Characteristics

Figure 3-1: Approved Memory List

Manufacturer Part Number	Description	Company
VL41B5263A-K9S	4GB 1333MHz unbuffered (SO-UDIMM)	Virtium
VL43B5263A-K9S	4GB 1333MHz registred (SO-RDIMM)	Virtium
VL41B5663A-F8S	2GB 1066MHz unbuffered (SO-UDIMM)	Virtium
VL41B2863F-F8S	1GB unbuffered (SO-UDIMM)	Virtium
VR7PU127258GBDK	4GB Modular 1 1333MHz unbuffered (SO-UDIMM)	Viking Modular
VL41B1G63A-K9S	8GB 1333MHz unbuffered (SO-UDIMM)	Virtium

3.4 Software

The AM4211 comes as a pre-installed system with all necessary OS, Filesystem, drivers and applications factory-installed with default configurations.

Updating the Software with a new Operating System or applications or new versions is provided by a dedicated update mechanism, which is described under the “Software Setup” section.

3.5 System Access

This section gives instructions for accessing the AM4211 using the Serial port via front plate connector.

3.5.1 Front Port Serial Connection

The OCTEON II processor’s serial console can be accessed directly via the front port connector with the appropriate cabling. The corresponding procedure is described below.

1 Connect the serial port on AM4211 front plate using the RS232 adapter, consult “RS232 Management Interface” section for more details .

Port settings are:

- 115 200 bps
- 8 bit, no parity, 1 stop bit (8N1)
- no flow control

2 Ensure that the board is powered up.

3 Wait for boot process to complete. Login is not required by default:

```
BusyBox v1.2.1 (2008.09.15-08:10+0000) Built-in shell (ash)
Enter 'help' for a list of built-in commands.

~ #
```

Chapter 4

Thermal Considerations

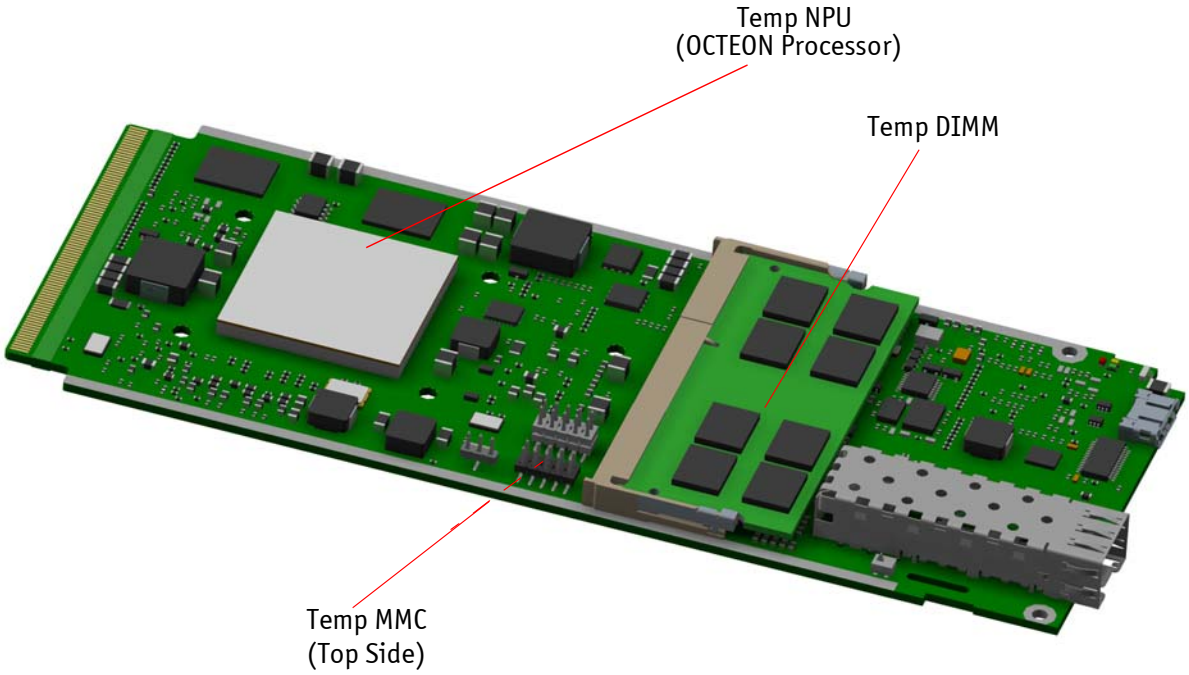
4. Thermal Considerations

4.1 Thermal Monitoring

To ensure optimal operation and long-term reliability of the AM4211, all onboard components must remain within the maximum temperature specifications. Operating the AM4211 above the maximum operating limits will result in permanent damage to the board. To ensure functionality at the maximum temperature, the Module Management Controller supports several temperature monitoring and control features.

The AM4211 includes three temperature sensors that are accessible via the Module Management Controller. Although temperature sensing information is made available to the MMC, the AM4211 itself does not provide any active means of temperature regulation.

Figure 4-1:Temperature Sensor Locations (AM4211 Top View, heat sinks not shown)



The Temp NPU is an on-chip sensor and the Temp MMC sensor is a diode located next to the MMC. The Temp DIMM sensor is a separate sensor measuring the temperature in the memory module. The Dual 10 GE Phy does not have a sensor. Simulations show that its temperature remains uncritical under operating conditions compared to the processor.

The following table shows the temperature thresholds of all three sensors.

Table 4-1:MMC Temperature Sensors Thresholds

Sensor	Lower Non Recoverable	Lower Critical	Lower Non Critical	Upper Non Critical	Upper Critical	Upper Non Recoverable
Temp DIMM	-8°C	0°C	5°C	70°C	75°C	98°C
Temp NPU	-6°C	0°C	5°C	85°C	90°C	101°C
Temp MMC	-8°C	0°C	5°C	60°C	65°C	72°C

Temperature values are measured with an accuracy of 1°C for the NPU and 3°C for the DIMM and the MMC.

4.2 External Thermal Regulation

The external thermal regulation of the AM4211 is realized using a dedicated heat sink design in conjunction with a system chassis that provides thermal supervision, controlled system airflow and thermal protection, such as increased airflow, reduced ambient air temperature, or power removal.

The main heat sink provided on the AM4211 has been specifically designed to ensure the best possible basis for operational stability and long-term reliability. The physical size, shape, and construction of the heat sink ensure the lowest possible thermal resistance. In addition, it has been specifically designed to efficiently support forced airflow concepts as found in modern AMC carriers and MicroTCA systems.

4.2.1 Forced Airflow

When developing applications using the AM4211, the system integrator must be aware of the overall system thermal requirements. All system chassis requirements must be provided to make sure they satisfy these requirements. As an aid to the system integrator, characteristic graphs are provided for the AM4211.

WARNING

As Kontron assumes no responsibility for any damage to the AM4211 or other equipment resulting from overheating any of the components, it is highly recommended that system integrators as well as end users confirm that the operational environment of the AM4211 complies with the thermal considerations set forth in this document.

4.2.2 Thermal Characteristic Graphs

The thermal characteristic graph shown in the following pages illustrates the maximum ambient air temperature as a function of the linear airflow rate for the power consumption indicated. The diagram is intended to serve as guidance for reconciling board and system, considering the thermal aspect. When operating below the indicated curves, the AMC runs steadily without any intervention of thermal supervision. When operated above the indicated curves, various thermal protection mechanisms may take effect eventually resulting in an emergency stop in order to protect the AMC from thermal destruction. In real applications this means that the board can be operated temporarily at a higher ambient temperature or at a reduced flow rate and still provide some margin for temporarily requested peak performance before thermal protection will be activated.

4.2.2.1 How to Read the Diagram

The diagram contains multiple curves displaying the thermal sensors temperature versus the provided airflow and the proper system class required. Full thermal load is not expected to be reached under real operating conditions. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, a safe operation is guaranteed. Above this operating point, the chassis thermal management must become active and take the necessary steps to protect the AMC from thermal destruction.

4.2.2.2 Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula:

Airflow = Volumetric flow rate / area.

The airflow is specified in m/s = meter-per-second or in LFM = linear-feet-per-minute, respectively.

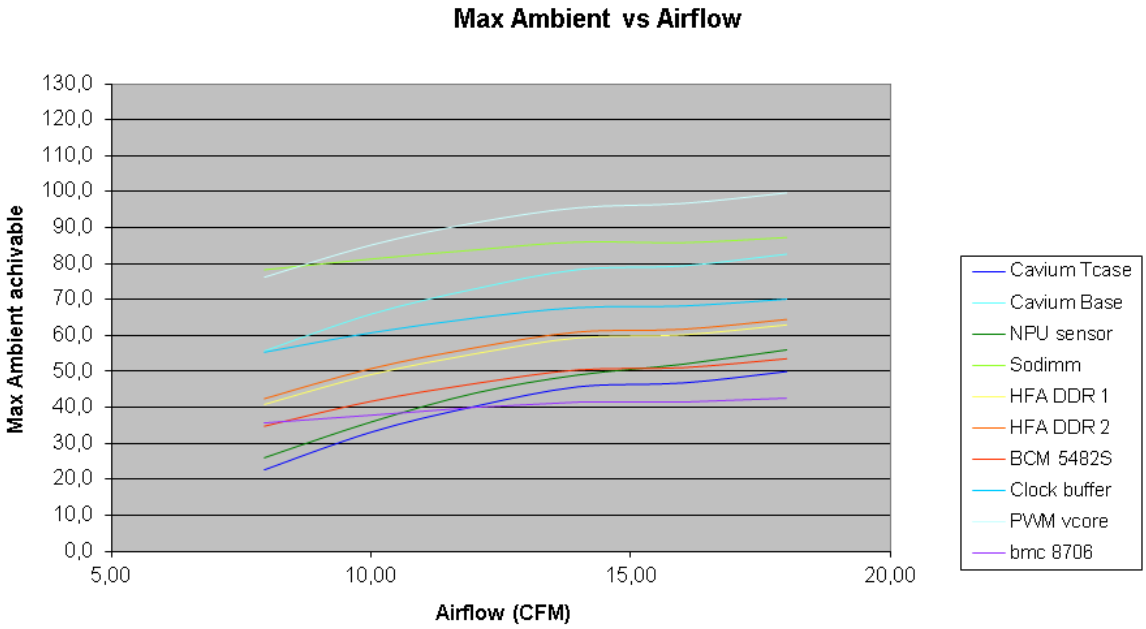
Conversion: 1 LFM = 0.00508 m/s; 1 m/s = 196.85 LFM

The following figure illustrates the operational limits of the AM4211 taking into consideration power consumption vs. ambient air temperature vs. airflow rate. The values are based on simulation data taking into account the actual power values of all components.

WARNING

In all situations, the maximum specified case temperature of the components must be kept below the maximum allowable temperature.

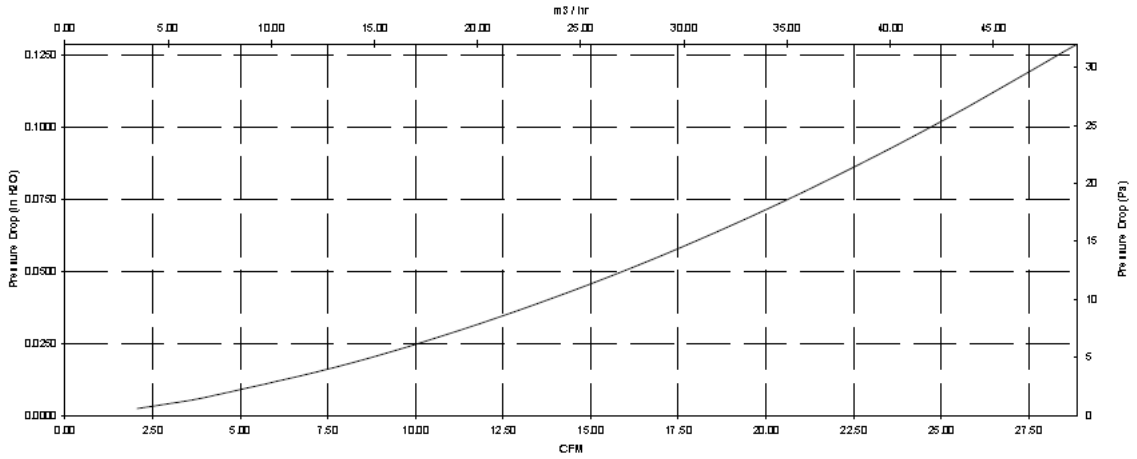
Figure 4-2:100% Operational Limits for the AM4211



4.2.3 Airflow Impedance

In order to determine the cooling requirements of the AM4211, the airflow impedance of the module has been determined via simulation. No card guides or struts have been used for the simulations because the resulting airflow impedance depends on individual configuration of the AMC carrier or MicroTCA system.

Figure 4-3:AM4211 Impedance Curve



4.2.4 Airflow Paths

The area between the front panel and the AMC Card-edge connector is divided into five zones, one I/O zone and four uniform thermal zones, A, B, C, and D. The PICMG AMC.0 Specification states that the uniformity of the airflow paths' resistance should provide an impedance on the A, B, C, and D zones that is within ± 25% of the average value of the four thermal zones.

Figure 4-4:Thermal Zones of the AM4211

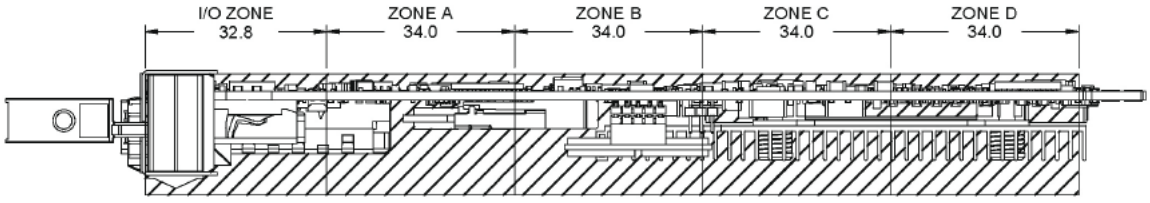


Table 4-2:Deviation of the Airflow Rate on the AM4211

Inlet Velocity			Deviation (%)			
CFM	m/s	LFM	ZONE A	ZONE B	ZONE C	ZONE D
2.3	0.28	55.6	-26.5	-12.7	22.8	16.4
3.4	0.42	82.8	-21.2	-14.1	20.9	14.4
4.5	0.56	110.0	-17.7	-15.2	19.3	13.6
9.0	1.11	219.1	-10.5	-16.8	15.3	12.0
13.6	1.68	329.7	-6.9	-17.0	12.8	11.0
18.3	2.25	442.4	-4.6	-16.6	11.0	10.1
22.9	2.82	555.1	-2.5	-15.6	9.2	8.9
27.6	3.40	668.8	-1.0	-15.1	7.9	8.2
32.3	3.98	782.5	0.1	-14.2	63.9	7.2

Chapter 5

Software Setup

5. Software Setup

5.1 MMC Firmware

The Module Management Controller (MMC) is a crucial component of any AMC module. Besides acting as a regular IPMI management controller (sensor monitoring, event generation, etc.), it also provides an interface to all necessary data related to module power requirements and implemented interfaces (E-Keying). Further, it plays an active role in the module hot swap state management. The carrier IPMI Controller (IPMC) communicates with the MMC using the local IPMB (IPMB-L) bus. In an ATCA/AMC environment, it is the IPMC that actually turns on/off module (payload) power. However, before the IPMC enables the module payload power, various criteria must be satisfied by both the carrier and the module, including handle switch state, power requirements and capabilities, matching interfaces, current module hot swap state, and any other special conditions as specified by the Shelf Manager policy.

5.1.1 Related Documentation

IPMI specifications: (http://www.intel.com/design/servers/ipmi/spec.htm)

- IPMI-Intelligent Platform Management Interface Specification. Second Generation v2.0, February 12, 2004 (part)
- IPMI- Platform Management FRU Information Storage Definition v1.0, Document Revision 1.1, September 1999

PICMG specifications: http://www.picmg.org

- PICMG® AMC.0 R2.0 - Advanced Mezzanine Card Base Specification
- PICMG® AMC.1 R1.0 - PCI Express and Advanced Switching on AdvancedMC
- PICMG® AMC.2 R1.0 – AMC Gigabit Ethernet/10 Gigabit XAUI Ethernet

Open tools documentation

- Ipmitool documentation: http://ipmitool.sourceforge.net
- OpenIPMI documentation: http://www.openipmi.sourceforge.net

The AM4211 is built in accordance to the AMC.0 R2.0 specification, and is also AMC.1 and AMC.2 compliant and is easily managed via IPMI v1.5/v2.0.

5.1.2 IPMI Sensors

The MMC includes many sensors for voltage or temperature monitoring and various others for pass/fail type signal monitoring.

Every sensor is associated with a Sensor Data Record (SDR). Sensor Data Records contain information about the sensors identification such as sensor type, sensor name and sensor unit. SDRs also contain the configuration of a specific sensor such as threshold/hystheresis, event generation capabilities that specifies sensor behavior. Some field of the sensor SDR are configurable through IPMI v1.5 command and are set to built-in initial values. The sensor also includes a field, identifying the sensor owner's address in the system. This allows the carrier to pre-pend an appropriate code when the SDR is scanned so the reader of the sensor list can determine which sensors belong to which physical board in the ATCA carrier or uTCA system.

From an IPMI perspective, the MMC is set up as a satellite management controller (SMC). It does support sensor devices, and uses the IPMI static sensor population feature of IPMI v1.5. All SDRs can be queried using Device SDR commands to the MMC.

The sensor name in its SDR has a name prefix which after module insertion is automatically adapted to the physical position of the module in a carrier or in a µTCA chassis. The format of this prefix is:

- in AMC bay 1...8 or µTCA slot 1...8: 'A1:', 'A2:', 'A3:', 'A4:', 'B1:', 'B2:', 'B3:', 'B4:'.
- in µTCA slot 9...12: 'C1:', 'C2:', 'C3:', 'C4:'.

Please note that in the case that the module is installed elsewhere, then the IPMB-L address of the module is unknown and the interface is off.

Module sensors that have been implemented are listed in the sensor list below.

Table 5-1:Sensor list

SDR ID	Name	Sensor Type Code	Reading Type Code	Description	Event Offset
0	IPMI Info-1	C0h (OEM Kontron)	70h (Discrete)	Internal Management Controller firmware diagnostic	
1	IPMI Info-2	C0h (OEM Kontron)	75h (Discrete)	Internal Management Controller firmware diagnostic	
2	FRU Agent	C5h (OEM Kontron FRU Info Agent State)	0Ah (Generic Discrete)	FRU Information Agent - FRU Data Error Detection	Offset 6: transition to Degraded Offset 8: Install Error
3	ModuleHotSwap	F2h (Module Hot Swap)	6Fh (Sensor Specific)	Refer to AMC.0 specification.	Offset 0: Module Handle Closed Offset 1: Module Handle Opened Offset 2: Quiesced Offset 3: Backend Power Failure Offset 4: Backend Power Shutdown Refer to AMC.0 R2.0 Section 3.6.6 Module Hot Swap Sensor.

SDR ID	Name	Sensor Type Code	Reading Type Code	Description	Event Offset
4	IPMBL State	C3h (OEM Kontron)	6Fh (Sensor Specific)	For additional information, refer to section Kontron IPMB-L Link	Offset 2: IPMB-L disabled Offset 3: IPMB-L enabled
5	MMC Stor Err	28h (Management Subsystem Health)	6Fh (Sensor Specific)	Generates an event when a local EEPROM storage error is detected.	Offset 1: Controller access degraded or unavailable See IPMI v1.5 table 36.3, Sensor type code 28h for sensor definition
6	MMC Reboot	24h (Platform Alert)	03h (Digital Discrete)	Generates an event when MMC reboot is detected.	Offset 0: State Deasserted Offset 1: State Asserted
7	MMC FWUP	C7h (Kontron OEM MC Firmware Upgrade Status)	6Fh (Sensor Specific)	Generates events after IPMI Firmware upgrade process is finished	Offset 0: Firmware upgrade in progress (no event) Offset 1: Firmware upgrade succeeded
8	MMC Ver Chg	2Bh (Version Change)	6Fh (Sensor Specific)	Generates an event when the IPMI FW changes	Offset 1: Firmware / Software change detected See IPMI v1.5 table 36.3, Sensor type code 2Bh (Version Change) for sensor definition
9	FPGA Ver Chg	2Bh (Version Change)	6Fh (Sensor Specific)	Generates an event when the IPMI FW changes	Offset 1: Firmware / Software change detected
10	IPMI Watchdog	23h (Watchdog 2)	6Fh (Sensor Specific)	OS Watchdog	Offset 0: Timer expired Offset 1: Board Reset Offset 2: Power Down Offset 3: Power Cycle Offset 8: Timer Interrupt See IPMI v1.5 table 36.3, Sensor type code 23h (Watchdog 2) for sensor definition
11	Board Reset	CFh (OEM Kontron Reset Sensor)	03h (Digital Discrete)	Type and source of Board Reset	Offset 0: Warm Reset Offset 1: Cold Reset See OEM sensor table, Sensor type code CFh for sensor definition
12	Temp MMC	01h (Temperature)	01h (Threshold Based)	Temperature Sensor of the outlet region	Sensor is only readable when Payload Power is on
13	Temp NPU	01h (Temperature)	01h (Threshold Based)	Temperature Sensor of the NPU	Sensor is only readable when Payload Power is on
14	Temp DIMM	01h (Temperature)	01h (Threshold Based)	Temperature Sensor of the DIMM memory)	Sensor is only readable when Payload Power is on.
15	Vcc +12V	02h (Voltage)	01h (Threshold Based)	Voltage on 12v board power supply	Sensor is only readable when Payload Power is on.
16	Vcc +5V	02h (Voltage)	01h (Threshold Based)	Voltage on 5v board power supply	Sensor is only readable when Payload Power is on.
17	Vcc +3.3V	02h (Voltage)	01h (Threshold Based)	Voltage on 3.3v board power supply	Sensor is only readable when Payload Power is on.

SDR ID	Name	Sensor Type Code	Reading Type Code	Description	Event Offset
18	Vcc +3.3V SUS	02h (Voltage)	01h (Threshold Based)	Voltage on 3.3v suspend (management) power supply	Sensor is only readable when Payload Power is on.
19	Vcc +2.5V	02h (Voltage)	01h (Threshold Based)	Voltage on 2.5v board power supply	Sensor is only readable when Payload Power is on.
20	Vcc +1.8V	02h (Voltage)	01h (Threshold Based)	Voltage on 1.8v board power supply	Sensor is only readable when Payload Power is on.
21	VCC +1.5V	02h (Voltage)	01h (Threshold Based)	Voltage on 1.5v board power supply	Sensor is only readable when Payload Power is on.
22	Vcc +1.2V	02h (Voltage)	01h (Threshold Based)	Voltage on 1.2v board power supply	Sensor is only readable when Payload Power is on.
23	Vcc +1.2V SUS	02h (Voltage)	01h (Threshold Based)	Voltage on 1.2v suspend	Sensor is only readable when Payload Power is on.
24	Vcc +1.1V	02h (Voltage)	01h (Threshold Based)	Voltage on 1.1v board power supply	Sensor is only readable when Payload Power is on.
25	Vcc +1.0V BCM	02h (Voltage)	01h (Threshold Based)	Voltage on 1.0v board power supply	Sensor is only readable when Payload Power is on.
26	Vcc VTT_DDR	02h (Voltage)	01h (Threshold Based)	Voltage on VTT_DDR board power supply	Sensor is only readable when Payload Power is on.
27	Vcc Vcore	02h (Voltage)	01h (Threshold Based)	Voltage on Vcore board power supply	Sensor is only readable when Payload Power is on.
28	Power Good	08h (Power Supply)	03h (Sensor Specific)	Power Good of the system	Offset 3: Power Supply Input Post See IPMI v1.5 table 36.3, Sensor type code 25h (Entity Presence) for definition
29	Health Error	24h (Platform Alert)	03h (Digital Discrete)	The sensor is an aggregation of analog sensors and shows the healthy state of the module. If the sensor is asserted, the health LED lit on amber	Offset 0: platform generated page Offset 1:platform generated LAN alert See IPMI v1.5 table 36.3, Sensor type code 27h (LAN) for definition
30	Memory Error	0Ch (Memory configuration Error)	6Fh (Digital Discrete)	Specify memory is not supported	Offset 7: Configuration error See IPMI v1.5 table 36.3, Sensor type code 24h for sensor definition
31	FPGA Error	24h (Platform Alert)	03h (Digital Discrete)	FPGA health status, assert when firmware is bad.	Offset 1:firmware bad See IPMI v1,5 table 36.3, Sensor type code 24h for sensor definition.
32	MMC SEL State	10h (Event Logging Disable)	6Fh (Sensor Specific)	Status of the system event log	Offset 2: Log area reset/ cleared Offset 4:SEL FULL Offset 5:SEL Almost FULL See IPMI v1.5 table 36.3, Sensor type code 10h (Event Log Disable)for definition

SDR ID	Name	Sensor Type Code	Reading Type Code	Description	Event Offset
33	Mod SFP	25h (Entity Present)	08h (Sensor specific)	The sensor shows presence or absence of SFP. No event is generated.	Offset 0: Entity Present Offset 1: Entity Absent Sensor is only readable when Payload Power is on.
34	SFP Link	27h (LAN)	6Fh (sensor Specific)	Status of the SFP Link	Offset 0: LAN Hearthbeat lost Offset 1: LAN Hearthbeat See IPMI v1.5 table 36.3, sensor type code 27h (LAN) for definition
35	GbE Link0	27h (LAN)	6Fh (sensor Specific)	Status of the GbE Link 0	Offset 0: LAN Hearthbeat lost Offset 1: LAN Hearthbeat See IPMI v1.5 table 36.3, sensor type code 27h (LAN) for definition
36	GbE Link1	27h (LAN)	6Fh (sensor Specific)	Status of the GbE Link 1	Offset 0: LAN Hearthbeat lost Offset 1: LAN Hearthbeat See IPMI v1.5 table 36.3, sensor type code 27h (LAN) for definition

5.1.2.1 OEM Sensor Description

5.1.2.1.1 Kontron FRU Info Agent

Table 5-2:Kontron FRU info agent sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
0Ah	C5h OEM Kontron FRU Info Agent	06h	Transition to degraded Event Data 2 is used a bit flag error Bit 7: unspecifiedError Bit 6: notPresentError Bit 5: multirecHeaderError Bit 4: multirecDataError Bit 3: timeout error Bit 2: ipmcError Bit 1: fruDataError Bit 0: commonHeaderError Event Data 3 is used a bit flag error Bit 7: reserved Bit 6: reserved Bit 5: SetPortState Not Supported Bit 4: SetPortState Error Bit 3: reserved Bit 2: reserved Bit 1: reserved Bit 0: Match Error, Not in single link matches
		08h	Install Error Event Data 2 is used a bit flag error Bit 7: unspecifiedError Bit 6: notPresentError Bit 5: multirecHeaderError Bit 4: multirecDataError Bit 3: timeout error Bit 2: ipmcError Bit 1: fruDataError Bit 0: commonHeaderError Event Data 3 is used a bit flag error Bit 7: SetClockState Not Supported Bit 6: SetClockState Error Bit 5: SetPortState Not Supported Bit 4: SetPortState Error Bit 3: Clock Internal Mismatch Bit 2: Clock Match Error, Not a single clock matches Bit 1: Internal mismatch Bit 0: Match Error, Not in single link matches

5.1.2.1.2 Kontron IPMB-L Link

Table 5-3:Kontron IPMB-L Link sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
6Fh	C3h OEM Kontron IPMB-L Link	02h	IPMB-L Disable Event Data 2: always 0 Event Data 3: bit[7:3]: always 0 bit [2:0]: 0h = no failure 1h = Unable to drive clock HI 2h = Unable to drive data HI 3h = Unable to drive clock LO 4h = Unable to drive data LO 5h = clock low timeout 6h = Under test (the IPM Controller is attempting to determine who is causing a bus hang) 7h = Undiagnosed Communication Failure
		03h	IPMB-L Enable Event Data 2: always 0 Event Data 3: bit[7:3]: always 0 bit [2:0]: 0h = no failure 1h = Unable to drive clock HI 2h = Unable to drive data HI 3h = Unable to drive clock LO 4h = Unable to drive data LO 5h = clock low timeout 6h = Under test (the IPM Controller is attempting to determine who is causing a bus hang) 7h = Undiagnosed Communication Failure

5.1.2.1.3 Kontron MMC Firmware Upgrade Status

Table 5-4:Kontron MMC FW upgrade status sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
6Fh	CAh OEM Kontron External Component Firmware Upgrade Status	00h	Firmware Upgrade in Progress (no event)
		01h	Firmware upgrade succeeded
		02h	Firmware upgrade failed

5.1.2.1.4 Kontron Reset

Table 5-5:Kontron reset sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
03h	CFh OEM Kontron RESET	00h 01h State Asserted / State Deasserted	Event Data 2: Reset Type 00h: Warm reset 01h: Cold reset 02h: Forced Cold [Warm reset reverted to Cold] 03h: Soft reset [Software jump] Event Data 3: Reset Source 00h: IPMI Watchdog [cold, warm or forced cold] (IPMI Watchdog2 sensors gives dditional details) 01h: IPMI commands cold, warm or forced cold] (chassis control, fru control) 02h: Processor internal checkstop 03h: Processor internal reset request 04h: Reset button [warm or forced cold] 05h: Power up [cold] 06h: Legacy Initial Watchdog / Warm Reset Loop Detection * [cold reset] 07h: Legacy Programmable Watchdog [cold, warm or forced cold] 08h: Software Initiated [soft, cold, warm of forced cold] 09h: Setup Reset [Software Initiated Cold] FFh: Unknown

5.1.2.1.5 Kontron User SW UpgradeStatus

Table 5-6:Kontron user SW upgrade status sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
6Fh	CAh OEM Kontron External Component Firmware Upgrade Status	00h	Firmware Upgrade in Progress (no event)
		01h	Firmware upgrade succeeded
		02h	Firmware upgrade failed

5.1.2.2 Sensor Thresholds

Following table shows sensor thresholds for voltages

Table 5-7:Voltage sensor thresholds

SENSOR Number / ID string	Lower Non-Recoverable	Lower critical	Lower non critical	Upper non critical	Upper critical	Upper Non-Recoverable
Vcc +3.3VSUS	2.802V	2.955V	-	-	3.623V	3.806V
Vcc +12V In	8.152V	9.826V	-	-	14.244V	15.918V
Vcc Vcore	0.987V	1.087V	-	-	1.165V	1.230V
Vcc +1.1V	0.971V	1.032V	-	-	1.170V	1.231V
Vcc +1.5V	1.321V	1.423V	-	-	1.579V	1.681V
Vcc +1.8V	1.062V	1.682V	-	-	1.920V	2.540V
Vcc VTT_DDR	0.643V	0.682V	-	-	0.821V	0.860V
Vcc +2.5V	2.197V	2.342V	-	-	2.660V	2.805V
Vcc +1.2V	0.907V	1.120V	-	-	1.312V	1.525V
Vcc +1.0V BCM	0.569V	0.932V	-	-	1.051V	1.414V
Vcc +3.3V	2.951V	3.093V	-	-	3.512V	3.654V
Vcc +1.2V SUS	1.053V	1.114V	-	-	1.289V	1.350V
Vcc +5V	4.126V	4.126V	-	-	5.597V	5.597V

Note:
Lower non critical and upper non critical values are not set to ensure no error in normal operation.

Note:
Vcc +1.8V Sensor is only monitored when the SyncE option is installed.

5.1.3 Field Replaceable Unit (FRU) Information

This FRU information contains the IPMI defined Board and Product Information areas that hold the part number and serial number of the board and the Multirecord Information Area that contains the PICMG defined Module Current Requirement Record, the AMC Point-to-Point Connectivity Record and the Clock Configuration Record.

The Internal Use Area is pre-allocated to 384 bytes and is free for customer use.

This FRU information responds to FRU ID #0, which is the ID for the MMC.

5.1.4 E-Keying

E-Keying has been defined in the AMC.0 Specification to prevent board damage, prevent wrong operation, and verify fabric compatibility. The FRU data contains the AMC Point-to-Point Connectivity record as described in Section 3.9 of the AMC.0 R2.0 specification.

When the Module is inserted in an ATCA AMC carrier or MicroTCA system, the carrier manager reads in the AMC Point-to-Point Connectivity record from FRU and determines whether the Board can enable the ports to the AMC connector. Set/Get AMC Port State IPMI commands defined by the AMC.0 specification are used for either granting or rejecting the E-keys.

5.1.5 Watchdog

The complete startup and execution process is guarded using external watchdog timers implemented by the hardware management subsystem IPMC. There are 4 distinct watchdog timers running during:

- boot initialization and early boot monitor execution
- boot monitor execution and preparation for OS loading
- OS execution and initialization

The watchdog timers will trigger a specific action when expired. The action is dependent on previous resets and on watchdog type.

The standard IPMI watchdog as implemented by the Linux IPMI driver supports different actions on watchdog timer expiry and a configurable watchdog pre-timeout.

This pre-timeout period is configurable from 1 second up. The pre-timeout allows application software to take actions just before the watchdog is triggered and causes a reset or error-halt-state. The pre-timeout action can either be configured to trigger a Linux kernel panic, where appropriate panic-handlers can collect data, or to inform a user-space application of the pre-timeout event.

5.1.6 MMC Firmware Code

MMC firmware code is organized into boot code and operational code, both of which are stored in a flash module. Upon an MMC reset, the MMC executes the boot code and performs the following:

- Self test to verify the status of its hardware and memory.
- Calculates a checksum of the operational code.

Upon successful verification of the operational code checksum, the firmware will jump to the operational code.

5.1.7 Updating MMC Firmware

Updating the MMC is possible in 2 different ways depending on the operating system running on the module. Those are:

- using ipmitool from the Linux shell (HPM.1 specification)
- IOL/Bridge + HPM

5.1.8 Override AMC.0 R2 support

Some carrier board are not AMC.0 R2 compliant.The AM4211 board firmware does not boot when Fat pipe is configured in PCIe mode.Use the following command to override AMC.0 R2:

- Override support of AMC.0 R2

```
# ipmitool raw 0x3e 0x20 0x18 0x1
```

- Enable support of AMC.0 R2 (default)

```
# ipmitool raw 0x3e 0x20 0x18 0x0
```

5.2 Board Firmware

The system is delivered with a bootloader and Linux OS preinstalled on the on-board 128MB NOR flash. The system will boot by default from this flash, which is directly connected to the bootbus of the Cavium OCTEON NPU. In addition to the on-board flash the board supports a mounted USB flash drive that can be used for application data. This USB flash drive is not used for booting in the default configuration.

The on-board flash is logically divided into two 64MB sections each consisting of 512 flash sectors. They are referred to as image0 and image1. The table 5-13 shows the physical addresses and associated flash sectors for each image once the board has booted on image 0.

Table 5-8:Fabric Default Flash Sector to Image Association

Physical Address Range	Linux MTD Partitions	Flash Sectors	Logical Image
0x17C00000 – 0x1BBFFFFF	mtd0 - mtd3	0 – 511	Image0
0x1BC00000 – 0x1FBFFFFF	mtd4 - mtd7	512 – 1023	Image1

Image0 and image1 can be swapped by a simple IPMI command. Physically, the uppermost address line of the flash device is inverted in this case. Flash sector to logical image association remains the same; however physical address to logical image association will be swapped as shown below.

Table 5-9:Swapped Flash Sector to Image Association

Physical Address Range	Linux MTD Partitions	Flash Sectors	Logical Image
0x17C00000 – 0x1BBFFFFF	mtd0-mtd3	512 – 1023	Image1
0x1BC00000 – 0x1FBFFFFF	mtd4 - mtd7	0 – 511	Image0

As the OCTEON NPU always starts booting from the first physical address in the flash, image0 system is started in the first case and image1 in the second.

After Linux startup, the flash is divided into 8 partitions (mtd0-mtd7) associated to the physical addresses as shown in the AM4211 partition scheme below. Note that association of MTD partitions to image depends on the started image as shown above.

Table 5-10:On-board 128 MB NOR Flash layout

Physical Address	Offset in flash	Size	Linux Partition	Designation	Description
0x17C00000	0	896KiB	mtd0	uboot	Active bootloader image
0x17CE0000	0xE0000	256KiB	mtd1	env	Active bootloader configuration variables
0x17D20000	0x120000	40960KiB	mtd2	kernel_rootfs	Active linux and Root file system
0x1A520000	0x2920000	23424KiB	mtd3	user_jffs2	Active user filesystem
0x1BC00000	0x4000000	896KiB	mtd4	uboot_backup	Backup bootloader
0x1BCE0000	0x40E0000	256KiB	mtd5	env_backup	Backup bootloader configuration variables
0x1BD20000	0x4120000	40960KiB	mtd6	kernel_rootfs_backup	Backup Linux and root filesystem
0x1E520000	0x6920000	23424KiB	mtd7	user_jffs2_backup	Backup user file system

When shipped from factory, image0 and image1 contain identical bootloader and firmware images and image0 system is booted by default. Image1 serves as a backup system which is started in case that image0 fails for some reason. It is recommended to always boot and work from image0 and leave image1 firmware untouched. This allows easy activation of the original firmware in case of any errors or corruption in the active image.

5.2.0.1 Image swap using bootloader predefined commands

The current firmware image is displayed during startup. It can be changed from the bootloader. Below are the available commands to change boot image. Those commands can be used in the U-Boot.

- Change to image 0

```
Kontron T5519# run activate_image0
```

- Change to image 1

```
Kontron T5519# run activate_image1
```

Using one of these commands, the board will immediately boot the selected image.

5.2.0.2 Image swap using ipmitool

Image swap can also be achieved using the ipmitool from the Linux shell of the board. The following command syntax must be used (IMAGE: 0 or 1):

```
~ # ipmitool raw 0x3e 0x20 0x00 <IMAGE>
```

It is possible to invoke the ipmitool with the same parameters from the AMC carrier that holds the AM4211 or even from external server provided that the ipmitool installed supports the Kontron OEM extensions.

However, the command must be invoked with appropriate bridging parameters set. E.g. on an AT8404 carrier with the AM4211 inside Bay 4, the syntax would be:

```
# ipmitool -b 7 -t 0x80 kontron boot set 0 0
```

Note:
In case that no ipmitool is available on a carrier or host server and image 0 has been corrupted, the board will perform an image swap automatically triggered by the system watchdog. An image swap is performed automatically by the MMC after the 3rd unsuccessful boot attempt (3 consecutive boot-up watchdog triggers)

5.2.1 Switching between Firmware Images

The IPMI command used for image swap can be executed either from the bootloader shell with a predefined script command or with a specific 'ipmitool' command either from the board itself, from an ATCA carrier or from an external server.

5.3 Bootloader

On the AM4211 Advanced Mezzanine Card (AMC), the bootloader 'u-boot' (universal bootloader) is used. The bootloader initializes the main components of the board like CPU, DDR3 RAM, serial lines etc. for operation and performs a power on self test (POST). After these steps have been finished, Linux kernel and application are started from flash. Bootloader used on the AM4211 is a modified version from u-boot version 2011.03 included in the OCTEON SDK 2.2. The following section describes most of the differences from the original u-boot that are used for the AM4211.

Generic u-boot features are not described in this section. Please read the u-boot documentation if the requested information is not describe in this section.

5.3.1 Bootloader shell and options

The boot process can be interrupted by typing the bootstopkey phrase "stop". This will open a bootloader command line interface.

Entering "?" provides a list of possible built-in commands, "printenv" provides a list of current environment settings. The bootloader shell can be used to customize boot options and system startup by changing some of its environment variables. A list of available environment variables and its description can be seen in the table below.

Table 5-11: Bootloader environment variables

Name	Type	Description
boardmacaddr	Var	Contains the default base MAC address for the OCTEON Ethernet interfaces. This variable is automatically set by the bootloader when the MAC address was read from the MMC/KCS interfaces. This should only be set manually when disable_kcs=yes or ignore_kcserr=yes to provide a "fallback" MAC address, when the KCS/MMC interface is not available or fails
bootcmd	Script	This variable defines a command string that is automatically executed when the initial countdown is not interrupted. This command is only executed when the variable bootdelay is also defined!
bootdelay	Var	After reset, U-Boot will wait this number of seconds before it executes the contents of the *bootcmd* variable. If the bootstopkey phrase is typed during this time, the bootloader command line interface is entered. Set this variable to *0* boots without delay. Be careful: depending on the contents of your *bootcmd* variable, this can prevent you from entering interactive commands again forever! Set this variable to *-1* to disable autoboot. default: 5 for flash based bootloader, -1 for RAM resident bootloader
kernel_rootfs_update	Script	Command script to flash a binary image transferred with tftpboot to the active image flash partition kernel_rootfs
kernel_rootfs_backup_update	Script	Command script to flash a binary image transferred with tftpboot to the backup image flash partition kernel_rootfs_backup
disable_kcs	Var	yes – completely disable all IPMI KCS access from bootloader <not set> - use KCS interface to retrieve MAC address and program watchdog et al (default)
ethact	Var	Default network interface used by network commands (bootp, tftpboot) default: octmgmt0
linuxcores	Var	Contains the number of CPU cores to allocate to the Linux kernel booted by the default boot commands default: 10
linuxmem	Var	Contains the amount of RAM in MB to allocate for the Linux kernel booted by the default boot comands default: 2048 (with a 2 Gig) 4096 (with a 4 Gig)
loadaddr	Var	Default load address for network transfers. This is used as a temporary storage for netbooting and firmware updates. default: 0x20000000
netretry	Var	<not set> – retry a failed netboot command infinitely with the interface defined by 'ethact' environment variable. no – do not retry failed net boot commands (bootp, tftpboot et al) using all available interfaces (default) yes – retry a failed netboot command by iterating through all available interfaces
nuke_user_jffs2	Script	Command script that erases the active image partition of the onboard flash partition user_jffs2
nuke_user_jffs2_backup	Script	Command script that erases the backup image partition of the onboard flash partition user_jffs2_backup
uboot_backup_update	Script	Command script to flash a U-Boot binary image transferred with tftpboot to the backup image bootloader
uboot_update / bootloaderupdate	Script	Command script to flash a U-Boot binary image transferred with tftpboot to the active image bootloader
watchdogboot	Var	0 – disable boot monitor watchdog (default) 5…n – timeout in seconds before boot monitor watchdog fires Note: This is the pBMWD watchdog

Name	Type	Description
watchdogos	Var	0 – disable OS load watchdog (default) 15…n – timeout in seconds before load OS watchdog fires Note: This is the pOSWD watchdog
ignoreposterr	Var	0 – stop boot process if power on self test errors are detected 1 – continue boot in the presence of power on self test errors (default)
postresult	Auto	Contains the power on self tests results: 0 - POST successful (default), 1 - POST failed
memtest	Var	0 = no DRAM test during POST 1 - quick DRAM test (default) 2 - full DRAM test
bootstopkey	Var	string to wait for during startup. If this string is entered, U-Boot will interrupt the boot process, stop the watchdog and will start its internal command line interface. default: “stop”

There are 3 different types of bootloader environment variables:

- **Script**: The variable is a set of consecutive (more simple) bootloader commands to perform a specific task. A command script is invoked using the ‘run <script>’ syntax. E.g. the ‘run nuke_env’ command would erase the bootloader environment sectors causing the bootloader to use its default environment upon next restart.
- **Var**: The variable controls a specific behavior of the bootloader startup sequence. E.g. the ‘bootdelay’ variable controls the time u-boot waits before execution of the bootcmd which normally loads and starts the Linux kernel.
- **Auto**: The variable is automatically set during bootloader startup sequence. E.g. the ‘postresult’ variable stores the result of the POST.

It is possible to modify environment variables and start the pre-defined scripts from the bootloader shell. It is strongly recommended not to modify the pre-defined script variables. However, definition and execution of user-defined script variables can be done.

CAUTION

Changing bootloader environment variables must be taken very carefully. It will change system behavior and can lead to a non-booting system

For additional information about u-boot, refer to http://sourceforge.net/projects/u-boot/

Modification of bootloader environment variables is done using the ‘setenv’ and ‘saveenv’ bootloader CLI commands. In the following example, the new environment script variable ‘bootcmdmyscript’ is defined. In addition, bootdelay is increased to 10. Finally, all changes are stored into flash environment sector.

```
Kontron T5519#  setenv bootcmdmyscript ‘bootp; tftpboot ${loadaddr} myimg.multi; bootm ${loadaddr}’
Kontron T5519#  setenv bootdelay 10
Kontron T5519#  saveenv
```

Environment changes are stored in the bootloader environment sectors. In case of failure (e.g. power loss), default setting are used and the following startup message is displayed:

```
Using default environment
```

Any changes of the environment can be cleared using the following commands:

```
Kontron T5519# env default -f
Kontron T5519# saveenv
```

5.3.2 Protected variables

Several variables are of great relevance for the system and are stored in a protected section of NVRAM. Some of these protected variables are, for example, the serial number of the module and the MAC addresses of the network interfaces, which are programmed during production and normally should not be changed.

5.3.3 NetConsole

If you are deploying a system, which has no UART connected to it, or is not practical to connect, you can use the network console. In U-Boot, the network console is implemented via the standard “devices” mechanism, which means that you can switch between the serial and network input/output devices by adjusting the 'stdin' and 'stdout' environment variables. To switch to the networked console, follow these instructions:

1 On AM4211, run the u-boot and enter the monitor shell

2 Setup network environment. For example:

```
LOCAL IP
# setenv ipaddr 192.168.100.2
# setenv netmask 255.255.255.0

HOST IP
# setenv gatewayip 192.168.100.1
# setenv serverip 192.168.100.1
# setenv ncip 192.168.100.1
```

3 To activate Netconsole, type the following command:

```
# run nc
```

4 On the host computer, create the “my_nc” script with the following content:

```
#! /bin/bash
[ $# = 1 ] || { echo "Usage: $0 target_ip" >&2 ; exit 1 ; }
TARGET_IP=$1
stty -icanon -echo intr ^T
nc -u -l 6666 < /dev/null &
nc -u ${TARGET_IP} 6666
stty icanon echo intr ^C
```

5 On the host computer, run network console startup script.

```
# ./my_nc 192.168.100.2
```

The U-Boot shell should be accessed

5.3.4 Booting Embedded Linux firmware from eUSB device

Follow these instructions to boot Cavium Embedded Linux from onboard USB mass-storage:

1 Make sure the USB mass-storage is formatted in FAT32 and copy any firmware to the USB mass-storage supported by board under test.

2 Connect to bootloader shell by entering the bootloader bootstop phrase ‘stop‘

3 Start the USB controller:

```
Kontron T5519# usb start
```

4 Copy the firmware file from the USB storage device to board memory:

```
Kontron T5519# fatload usb 0:1 0x20000000 [firmware_file]
```

5 Start the new firmware from memory:

```
Kontron T5519# bootoctlinux 0x20000000 numcores=${linuxcores} mem=${linuxmem} con-
sole=ttyS0,${baudrate} ${mtdparts} ${bootargs}
```

5.3.5 U-boot memory configurations

Some of the memory configurations need to be done manually using u-boot environment variables.

The following are the possible memory configurations:

1 Configuring the DDR clock / data rate:

```
Kontron T5519# setenv ddr_clock_hertz [CLOCK]
   [CLOCK] = DDR clock in hertz, the real data rate will be de double of this value.
   Here is an example:
Kontron T5519# setenv ddr_clock_hertz 533333333
  Will configure the DDR clock at 533Mhz, the data rate will be 1066Mhz.
Kontron T5519# setenv ddr_clock_hertz 666666666
  Will configure the DDR clock at 666Mhz, the data rate will be 1333Mhz.
```

2 Configuring the memory window used in Linux environment:

```
Kontron T5519# setenv linuxmem [SIZE]
   [SIZE] = size of memory in megabytes, here is an example:
Kontron T5519# setenv linuxmem 2048M
  Will configure a memory window of 2GB for Embedded Linux.
```

5.3.6 Network interfaces

The following table represents the logical u-boot network interfaces related to their physical Cavium connection (QLM):

Table 5-12:Bootloader network interfaces

AMC Port	Cavium physical interfaces (QLM)	u-boot logical name(s)
0	RGMII 0	octmgmt0
1	RGMII1	octmgmt1
8 to 11	QLM1 / XAUI	octeth1
8	QLM1 / SGMII Lane 0	octeth1
9	QLM1 / SGMII Lane 1	octeth2
10	QLM1 / SGMII Lane 2	octeth3
11	QLM1 / SGMII Lane 3	octeth4
Front SFP	QLM2 / 1000Base-X	octeth0
Front SFP+	QLM2 / 10GbE	octeth0

U-Boot automatically sets the variable **ethact** to the name of the Ethernet interface that is currently active (default: octmgmt0). This variable can be changed on host to force U-Boot to use a different network interface.

5.3.7 Bootloader Update

To update the bootloader, the new U-boot binary is transferred to the board using TFTP. After that, this binary is written into the onboard flash. The internal controller is used for network connection.

Prerequisites: a working TFTP server, DHCP server and network connectivity to the DHCP and TFTP server. The new bootloader image has to be stored on the TFTP server. No jumper settings are required on the AM4211.

There is one possible way to update the bootloader image and it's by using the predefined update scripts from the bootloader CLI. It is recommended to always update firmware of the active image. In case of a failure, it is possible to restore the board using the still unchanged redundant image. After the updated firmware is running properly, the redundant image can be updated to the same version, only if it is required.

The following procedure defines the update of the image 0 bootloader:

- Start system and connect to serial console
- Connect to bootloader shell by entering the bootloader bootstop phrase 'stop'

```
U-Boot 2011.03-KCI-0.42 (Development build, svnversion: u-boot:exported, exec:) (Build time:
Mar 12 2012 - 13:56:25)

Skipping PCIe port 0 BIST, in EP mode, can't tell if clocked.
Skipping PCIe port 1 BIST, reset not done. (port not configured)
BIST check passed.
DFM interface initialized 512 MB
KONTRON_T5519 FPGA version: 14 Revision: 3
Reset Type: 01 cold reset, Source: 08 Software Initiated
KONTRON_T5519 board revision major:3, minor:0
```

```
OCTEON CN6645-AAP pass 1.2, Core clock: 1100 MHz, IO clock: 800 MHz, DDR clock: 533 MHz (1066
Mhz data rate)
Base DRAM address used by u-boot: 0x4f800000, size: 0x800000
DRAM: 1 GiB
Clearing DRAM...... done
KCS: Reading boot image number      : Image 0
KCS: Reading front SFP settings     : Front SFP GE
KCS: Reading fat pipe settings      : Port 4-7 = Target PCIe, Port 8-11 = Disable
KCS: Reading PCIe clock source      : external FCLKA
KCS: Reading ethaddr                : 00:a0:a5:78:5d:74
KCS: Reading serial#                : 9009096065
KCS: Reading Power throttling       : CORE0:70 CORE1:70 CORE2:70 CORE3:70 CORE4:70
                                    : CORE5:70 CORE6:70 CORE7:70 CORE8:70 CORE9:70
Flash: 128 MiB
PCIe: Port 0 in endpoint mode.
PCIe: Port 1 is unknown, skipping.
PCI console init succeeded, 1 consoles, 1024 bytes each
Net:   Bcm8707: probed
octmgmt0, octmgmt1, octeth0
USB:   USB EHCI 1.00
scanning bus for devices... 1 USB Device(s) found
Type the command 'usb start' to scan for USB storage devices.

autoboot in 5 seconds...
press 'stop' phrase to abort <==== Enter 'stop' now
IPMI watchdog stopped
Kontron T5519#
```

- Get proper network settings

```
Kontron T5519# dhcp
```

- Update U-Boot

```
Kontron T5519# tftp ${loadaddr} u-boot-kontron_t5519-0.42.bin
Kontron T5519# bootloaderupdate
Kontron T5519# reset
```

5.3.8 Embedded Linux update

1 Start system and connect to serial console

2 Connect to bootloader shell by entering the bootloader bootstop phrase 'stop'

3 Get proper network settings

```
Kontron T5519# dhcp
```

4 Update Embedded linux to version x.xx. Below is an example (kernel_rootfs is the first bank):

```
Kontron T5519# tftpboot ${loadaddr} vmlinux.64-kontron_t5519_0.42
Kontron T5519# run kernel_rootfs_update
Kontron T5519# reset
```

5.4 Embedded Linux

5.4.1 Embedded filesystem and init script customizations

The embedded Linux file system on the AM4211 is an initramfs. This means that any file can be modified but will return to their original states after a Cavium NPU restart.

By default there is a flash partition that is automatically mounted to /mnt. This partition can be used to have permanent R/W storage space. All data stored in /mnt will be permanently saved to the flash (user_jffs2, /dev/mtd3).

You can also creating custom initialization script by adding this in the user_jffs2 partition (/mnt):

```
# mkdir /mnt/etc
# vi /mnt/etc/rc.local
```

Add your init code in this file (shell script).

```
# chmod +x /mnt/etc/rc.local
```

The script file /mnt/etc/rc.local will be executed at the end of each boot.

5.4.2 Access to NFS share from Cavium Embedded Linux

There is no portmap included in Cavium embedded Linux. To mount NFS share you need to disable the locking mechanism with the -o arguments, here is an example:

```
# mount -o nolock [SHARE_ADDRESS] [MOUNT_POINT]
```

5.4.3 eUSB Storage

The optional eUSB storage can be used into the Linux environment. To mount the device, use the following commands:

```
# mkdir /mnt/usb
# mount /dev/sda1 /mnt/usb
```

5.4.4 Booting over PCI (oct-remote-boot)

Octeon can be booted from a remote host without the need for a boot flash on the Octeon board. For PCI targets, the Octeon board must be configured for PCI boot mode. This keeps all cores in reset after the chip is taken out of reset.

1 With cfgtool, select one of the following modes:

```
[23] Port 4-7 = Target PCIe, Port 8-11 = Disable     ( BOOT_PCIE )
[24] Port 4-7 = Target PCIe, Port 8-11 = Target PCIe ( BOOT_PCIE )
[25] Port 4-7 = Target PCIe, Port 8-11 = LAN - XAUI  ( BOOT_PCIE )
[26] Port 4-7 = Target PCIe, Port 8-11 = LAN - SGMII ( BOOT_PCIE )
```

Power cycle the PCIe Host board.

2 On the PCIe Host board, use <lspci> and validate that the AM4211 is present in the displayed list

```
0f:00.0 MIPS: Cavium Networks Unknown device 0092 (rev ff)
```

3 On the PCIe Host board, go to the remote-utils folder of the Cavium SDK.

```
cd <Cavium SDK>/host/remote-utils
```

4 Configure the remote protocol env variable

```
export OCTEON_REMOTE_PROTOCOL=PCI
```

5 Start U-boot on AM4211

```
./oct-remote-boot --board=generic --ddr0spd=0x50 --ddr_clock_hz=5333333333 u-boot-kontron_t5519.bin
```

Note:

To disable the Boot PCIe mode, use the one of the following method:

From the Host Board:

```
# ipmitool -m 0x20 -t 0x7a -b 7 raw 0x3e 0x20 2 0
```

From the AM4211 u-boot shell:

```
# kcs raw 0x3e 0x20 2 0
```

From the AM4211 linux shell:

```
# ipmitool raw 0x3e 0x20 2 0
# cfgtool -p 0 -s -c
```

Please refer to the online documentation provided with the Cavium Networks SDK for more details.

5.4.5 Onboard flash access within Cavium Embedded Linux

The Linux environment use MTD support to access the Flash device, here are the MTD partitions:

Table 5-13:Embedded Linux MTD partitions

Flash logical name	Descriptions	Partitions address Size
uboot	Active bootloader	/dev/mtd0
env	Active bootloader configuration	/dev/mtd1
kernel_rootfs	Active Linux et Root filesystem	/dev/mtd2
user_jffs2	Active User filesystem	/dev/mtd3
uboot_backup	Backup bootloader	/dev/mtd4
env_backup	Backup bootloader configuration	/dev/mtd5
kernel_rootfs_backup	Backup Linux et Root filesystem	/dev/mtd6
user_jffs2_backup	Backup User filesystem	/dev/mtd7

5.4.6 Ethernet over Serial Rapid IO

Linux has an Ethernet device for each of the four standard Rapid IO mailboxes. The following Ethernet interfaces are available through «ifconfig».

- rio0 = Interface 0, send/receive on mailbox 0
- rio1 = Interface 0, send/receive on mailbox 1
- rio2 = Interface 0, send/receive on mailbox 2
- rio3 = Interface 0, send/receive on mailbox 3

Since the Rapid IO transport is different from the expected ethernet transport, these devices treat MAC addresses specially. Extra data describing the Rapid IO message header fields is encoded into the destination MAC address. The format of the MAC address is:

Table 5-14:SRIO MAC adress

Byte	Bits	Description
0-3	31:0	Must be zero.
4-5	15:0	16 bits for the SRIO destination ID.

Please refer to the online documentation provided with the Cavium Networks SDK for more details.

5.5 Using CFGTOOL

cfgtool is a central configuration software included in the embedded firmware of the AM4211. This software perform the low-level configuration of the AM4211 including updating the FRU data to reflect the selected configuration.

What cfgtool can do:

- Configure the QLM interfaces connected to the backplane.
- Configure the PCI-express clock source of the QLM interfaces.
- Configure the SFP+ front interface mode.
- Configure power throttling of the Cavium processor.

5.5.1 Usage

```
cfgtool [--help|-h][--status|-t][--interface|-i][--fatpipe|-p][--clock|-k]
        [--power|-w][--core0|-0][--core1|-1]
        [--core2|-2][--core3|-3][--core4|-4][--core5|-5]
        [--core6|-6][--core7|-7][--core8|-8][--core9|-9]
```

[--set|-s][--cycle|-c][--nofru|-n]
[--debug|-d]
-h Show possible settings available for this board
-t Show current running configuration
-i <num> Interface setting
-p <num> Fatpipe setting
-k <num> Clock setting
-w <pwr> AMC optimized power (Watts)
-0 <pwr> Core 0 power throttle (%)
-1 <pwr> Core 1 power throttle (%)
-2 <pwr> Core 2 power throttle (%)
-3 <pwr> Core 3 power throttle (%)
-4 <pwr> Core 4 power throttle (%)
-5 <pwr> Core 5 power throttle (%)
-6 <pwr> Core 6 power throttle (%)
-7 <pwr> Core 7 power throttle (%)
-8 <pwr> Core 8 power throttle (%)
-9 <pwr> Core 9 power throttle (%)
-s Set configuration (change HW setting and update ekeying info)
-c Perform power cycle of payload power to activate settings
-n No FRU data modification
-d Debug flag
-V Version information

5.5.1.1 Detailed Description of the Options

-h | --help

This option shows a list of possible settings.

```
~ # cfgtool -h
Config Options for [3] AM4211/T5519, Rev 2 CN66XX

[--interface|-i <num>]
  [0] Front SFP XAUI
  [1] Front SFP GE

[--fatpipe|-p <num>]
  [ 0] Port 4-7 = Disable,     Port 8-11 = Disable
  [ 1] Port 4-7 = Disable,     Port 8-11 = Target PCIe
  [ 2] Reserved
  [ 3] Port 4-7 = Disable,     Port 8-11 = Host PCIe
  [ 4] Port 4-7 = Disable,     Port 8-11 = LAN - XAUI
  [ 5] Port 4-7 = Disable,     Port 8-11 = LAN - SGMII
  [ 6] Port 4-7 = Target PCIe, Port 8-11 = Disable
  [ 7] Port 4-7 = Target PCIe, Port 8-11 = Target PCIe
  [ 8] Port 4-7 = Target PCIe, Port 8-11 = LAN - XAUI
  [ 9] Port 4-7 = Target PCIe, Port 8-11 = LAN - SGMII
  [10] Port 4-7 = Host PCIe,   Port 8-11 = Disable
  [11] Port 4-7 = Host PCIe,   Port 8-11 = Host PCIe
  [12] Port 4-7 = Host PCIe,   Port 8-11 = LAN - XAUI
  [13] Port 4-7 = Host PCIe,   Port 8-11 = LAN - SGMII
  [14] Port 4-7 = Target sRIO, Port 8-11 = Disable
  [15] Port 4-7 = Target sRIO, Port 8-11 = Target PCIe
  [16] Reserved
  [17] Port 4-7 = Target sRIO, Port 8-11 = LAN - XAUI
  [18] Port 4-7 = Target sRIO, Port 8-11 = LAN - SGMII
  [19] Port 4-7 = Host sRIO,   Port 8-11 = Disable
  [20] Port 4-7 = Host sRIO,   Port 8-11 = Host PCIe
  [21] Port 4-7 = Host sRIO,   Port 8-11 = LAN - XAUI
  [22] Port 4-7 = Host sRIO,   Port 8-11 = LAN - SGMII
```

```
  [23] Port 4-7 = Target PCIe, Port 8-11 = Disable     ( BOOT_PCIE )
  [24] Port 4-7 = Target PCIe, Port 8-11 = Target PCIe ( BOOT_PCIE )
  [25] Port 4-7 = Target PCIe, Port 8-11 = LAN - XAUI  ( BOOT_PCIE )
  [26] Port 4-7 = Target PCIe, Port 8-11 = LAN - SGMII ( BOOT_PCIE )

[--clock|-k <num>]
  [0] Local Clock
  [1] External FCLKA

[--power|-w <pwr>]
  [20-40] AMC Optimized Power Value in Watts

[--core0|-0 <pwr>]
  [10-100] Core Power Throttle in %

[--core1|-1 <pwr>]
  [10-100] Core Power Throttle in %

[--core2|-2 <pwr>]
  [10-100] Core Power Throttle in %

[--core3|-3 <pwr>]
  [10-100] Core Power Throttle in %

[--core4|-4 <pwr>]
  [10-100] Core Power Throttle in %

[--core5|-5 <pwr>]
  [10-100] Core Power Throttle in %

[--core6|-6 <pwr>]
  [10-100] Core Power Throttle in %

[--core7|-7 <pwr>]
  [10-100] Core Power Throttle in %

[--core8|-8 <pwr>]
  [10-100] Core Power Throttle in %

[--core9|-9 <pwr>]
  [10-100] Core Power Throttle in %
```

-t | --status

This option shows the present configuration stored in NVRAM of the MMC. This setting will take effect after invoking a "Chassis Control Power cycle" command or after a complete hotswap cycle with remove and reinsertion of the module.

```
~ # cfgtool -t
Getting Current Settings...
================================================================================
Board Type: [3] AM4211/T5519, Rev 2 CN66XX
Image     : [1] Image 1
================================================================================
Current Setting:
--------------------------------------------------------------------------------
Interf.: [0] Front SFP XAUI
Fatpipe: [19] Port 4-7 = Host sRIO,   Port 8-11 = Disable
CLK    : [0] Local Clock
Power  : 39.60 Watt
Core 0 : 100%
Core 1 : 100%
```

```
Core 2 : 100%
Core 3 : 100%
Core 4 : 100%
Core 5 : 100%
Core 6 : 100%
Core 7 : 100%
Core 8 : 100%
Core 9 : 100%
================================================================================
```

-I | --interface <INTF>

This option configures the FRONT SFP+ interface.

This option checks if the setting <INTF> is possible for this board.

To set this setting the **[-s|--set]** option has to be appended.

Possible configurations are:

0 XAUI, 10G Optical fiber.
1 GE, 1G copper.

-p | --fatpipe <num>

This option configures the QLM0/1 connected to the AMC connector.

Possible configurations are:

[0] Port 4-7 = Disable, Port 8-11 = Disable
[1] Port 4-7 = Disable, Port 8-11 = Target PCIe
[2] Reserved
[3] Port 4-7 = Disable, Port 8-11 = Host PCIe
[4] Port 4-7 = Disable, Port 8-11 = LAN - XAUI
[5] Port 4-7 = Disable, Port 8-11 = LAN - SGMII
[6] Port 4-7 = Target PCIe, Port 8-11 = Disable
[7] Port 4-7 = Target PCIe, Port 8-11 = Target PCIe
[8] Port 4-7 = Target PCIe, Port 8-11 = LAN - XAUI
[9] Port 4-7 = Target PCIe, Port 8-11 = LAN - SGMII
[10] Port 4-7 = Host PCIe, Port 8-11 = Disable
[11] Port 4-7 = Host PCIe, Port 8-11 = Host PCIe
[12] Port 4-7 = Host PCIe, Port 8-11 = LAN - XAUI
[13] Port 4-7 = Host PCIe, Port 8-11 = LAN - SGMII
[14] Port 4-7 = Target sRIO, Port 8-11 = Disable
[15] Port 4-7 = Target sRIO, Port 8-11 = Target PCIe
[16] Reserved
[17] Port 4-7 = Target sRIO, Port 8-11 = LAN - XAUI
[18] Port 4-7 = Target sRIO, Port 8-11 = LAN - SGMII
[19] Port 4-7 = Host sRIO, Port 8-11 = Disable
[20] Port 4-7 = Host sRIO, Port 8-11 = Host PCIe
[21] Port 4-7 = Host sRIO, Port 8-11 = LAN - XAUI
[22] Port 4-7 = Host sRIO, Port 8-11 = LAN - SGMII
[23] Port 4-7 = Target PCIe, Port 8-11 = Disable (BOOT_PCIE)
[24] Port 4-7 = Target PCIe, Port 8-11 = Target PCIe (BOOT_PCIE)
[25] Port 4-7 = Target PCIe, Port 8-11 = LAN - XAUI (BOOT_PCIE)
[26] Port 4-7 = Target PCIe, Port 8-11 = LAN - SGMII (BOOT_PCIE)

To set this setting, the **[-s|--set]** option has to be appended.

-X | --core <0-100%>

This option configures the Maximum power usage for each core of the the Cavium processor.

To set this setting, the **[-s|--set]** option has to be appended.

-w | --power <20-40 WATTS>

This option configures the maximum power budget for the AM4211.

To set this setting, the **[-s|--set]** option has to be appended.

```
Power(w) Throttling(%)
------------------------
<20W 10%
20W 10%
27,5W 100%
>27,5W 100%
Power = (Throttling + 230) / 12
```

-k | --clock <CLOCK>

This option configures the QLM0/1 clock reference source.

Possible configurations are:

0 QLM0/1 use local AMC clock.
1 QLM0/1 use external FCLKA signal from the AMC connector.

Note:
FCLKA input may be damaged if driven by an M-LVDS driver.

To set this setting the **[-s|--set]** options has to be appended.

-s | --set

This option sets the configuration in the MMCs NV ram, updates the FRU data multirecord and performs a MMC reset (IPMI Cold Reset).

-c | --cycle

This option send the IPMI command "Chassis control Power cycle" to the MMC to perform a payload power cycle. During the power cycle the configuration will be enabled. This option is allowed without any other options or when a valid PCIe or Interface setting is configured and activated with the **[-s|--set]** option.

-n | --nofru

This option prevent FRU data update when changing an interface.

-d | --debug

This option sets the debug level. If this option is used twice the debug level is increased.

5.6 Cavium Linux BSP

This package includes the required modifications to the OCTEON SDK 2.2.0 to support Kontron AM4211 device.

5.6.1 Requirements

- Linux operating system (tested with Redhat Linux Enterprise 5.4).

- Full Octeon SDK version 2.2.0

- Update to SDK 2.2.0 - patch level 1

5.6.2 Install Instructions

1 Perform the full installation of Octeon SDK 2.2.0.

```
OCTEON-SDK-2.2.0-414.i386.rpm
OCTEON-LINUX-2.2.0-414.i386.rpm
```

2 Perform installation of Update to SDK 2.2.0 - patch level 1

```
sdk_2.2.0_update_p1.tgz
```

3 Go to Octeon SDK directory and install all Kontron patches included:

```
# cd [OCTEON_SDK]
# patch -p1 < T5519-bootloader_0.42.patch
# patch -p1 < T5519-executive_0.42.patch
# patch -p1 < T5519-linux_0.42.patch
```

4 Copy ipmitool

```
# cp ipmitool-1.8.11-K26.tar.gz [OCTEON_SDK]/linux/embedded_rootfs/storage
```

5 Copy watchdog

```
# cp watchdog-5.8.tar.gz [OCTEON_SDK]/linux/embedded_rootfs/storage
```

5.6.3 Build

1 Go to OCTEON SDK directory and configure the SDK environment :

```
# source env-setup OCTEON_CN66XX_PASS1_2
```

2 Set the build subversion, here is an example :

```
# export U_BOOT_BUILD_NUMBER_STR="-KCI 0.34"
# export KONTRON_CONFIG_LOCAL_VERSION=-0.34
```

3 Build U-boot binary

```
# cd [OCTEON_SDK]/bootloader/u-boot
# make kontron_t5519_config
# make
```

The generated file is [OCTEON_SDK]/bootloader/uboot/u-boot-kontron_t5519.bin

4 Build linux kernel and root file system :

```
# cd [OCTEON_SDK]/linux
# make kernel
# make strip
```

The generated file is [OCTEON_SDK]/linux/kernel2.6/linux/vmlinux.64

Please refer to the online documentation provided with the Cavium Networks SDK for more detail.

5.6.4 Simple executive applications

Building simple executive applications requires the availability of the Cavium Networks SDK which must be obtained from Cavium Networks directly. The Cavium Networks SDK includes OCTEON Executive Library as well as documentation and examples for OCTEON simple executive development. The OCTEON Executive Library provides runtime support, hardware abstraction, memory management, and synchronization routines for the OCTEON processor. It is composed of the libcvmx.a library as well as header files that provide a lot of functionality with inline functions. The Executive is designed to provide an efficient environment for developing data plane code for OCTEON. It supports a single thread of execution per cnMIPS core.

Simple executive applications can be used without the support of an OS, however, memory TLBs for each core must have been set up correctly before starting a SE. This is done by the bootloader ‘bootoct’ command which is part of the OCTEON u-boot port.

Please refer to the online documentation provided with the Cavium Networks SDK for more detail.

Refer to previous section for the procedure to install the SDK.

- Build the ‘passthrough’ sample application

```
# make –C examples/passthrough
```

A. Connectors Pinouts

A.1 USB SSD Flash Module

Signal	Pin Number	Signal	Pin Number
V_5V	1	NC	2
USB DATA (-)	3	NC	4
USB DATA (+)	5	NC	6
GND	7	NC	8
NC (KEY)	9	NC	10

A.2 SFP+ Front IO

Pin Number	Signal	Pin Number	Signal
20	VeeT	1	VeeT
19	TD-	2	Tx Fault
18	TD+	3	Tx Disable
17	VeeT	4	SDA
16	VccT	5	SCL
15	VccR	6	SFP Present #
14	VeeR	7	Rate Select 0
13	RD+	8	LOS
12	RD-	9	Rate Select 1
11	VeeR	10	VeeR

A.3 Serial Port Pinout

Signal	Pin
N.C.	1
RXD #	2
TXD#	3
DTR	4
GND	5
DSR	6
RTS	7
CTS	8
N.C.	9
N.C.	10

B. Getting Help

If, at any time, you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, contact our Technical Support at:

North America	EMEA
Tel.: (450) 437-5682	Tel.: +49 (0) 8341 803 333
Fax: (450) 437-8053	Fax: +49 (0) 8341 803 339

If you have any questions about Kontron, our products, or services, visit our Web site at: www.kontron.com

You also can contact us by E-mail at:

North America: support@ca.kontron.com

EMEA: support@kontron-modular.com

Or at the following address:

North America	EMEA
Kontron Canada, Inc.	Kontron Modular Computers GmbH
4555, Ambroise-Lafortune	Sudetenstrasse 7
Boisbriand, Québec	87600 Kaufbeuren
J7H 0A4 Canada	Germany

B.1 Returning Defective Merchandise

Before returning any merchandise please do one of the following:

- Call

    1 Call our Technical Support department in North America at (450) 437-5682 and in EMEA at +49 (0) 8341 803 333. Make sure you have the following on hand: our Invoice #, your Purchase Order #, and the Serial Number of the defective unit.

    2 Provide the serial number found on the back of the unit and explain the nature of your problem to a service technician.

    3 The technician will instruct you on the return procedure if the problem cannot be solved over the telephone.

    4 Make sure you receive an RMA # from our Technical Support before returning any merchandise.

- E-mail

    1 Send us an e-mail at: RMA@ca.kontron.com in North America and at: orderprocessing@kontron-modular.com in EMEA. In the e-mail, you must include your name, your company name, your address, your city, your postal/zip code, your phone number, and your e-mail. You must also include the serial number of the defective product and a description of the problem.

B.2 When Returning a Unit

- In the box, you must include the name and telephone number of a contact person, in case further explanations are required. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.
- Ensure that the unit is properly packed. Pack it in a rigid cardboard box.
- Clearly write or mark the RMA number on the outside of the package you are returning.
- Ship prepaid. We take care of insuring incoming units.

North America	EMEA
Kontron Canada, Inc.	Kontron Modular Computers GmbH
4555, Ambroise-Lafortune	Sudetenstrasse 7
Boisbriand, Québec	87600 Kaufbeuren
J7H 0A4 Canada	Germany

C. Glossary

Acronyms	Descriptions
ACL	Access Control List. IP Access Control List.
ACPI	Advanced Configuration & Power Interface
AdvancedMC	(Same as AMC). Advanced Mezzanine Card.
AMC	(Same as AdvancedMC). Advanced Mezzanine Card.
AMC.0	Advanced Mezzanine Card Base Specification.
AMC.1	PCI Express and Advanced Switching on AdvancedMC. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0).
AMC.2	Ethernet Advanced Mezzanine Card Specification. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0).
AMC.3	Advanced Mezzanine Card Specification for Storage. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0).
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
APM	Advanced Power Management
ARMD	ATAPI Removable Media Device
ARP	Address Resolution Protocol
ASCII	American Standard Code for Information Interchange. ASCII codes represent text in computers, communications equipment, and other devices that work with text.
ASF	Alert Standard Format. A standard for how alerting and remote-control capabilities on network controllers work.
ATCA	Advanced Telecommunications Computing Architecture
BCD	Binary-Coded Decimal
BER	Bit Error Ratio
BI	Base Interface. Backplane connectivity defined by the ATCA.
BMC	Base Management Controller
BT	Block Transfer. An optional IPMI system management interface.
CB	Certification Body
CCB	Core Complex Bus (Inside PowerQuicc III CPU)
CFM	Cubic Foot per Minute
CLI	Command-Line Interface
CLK1	AdvancedTCA bused resource Synch clock group 1
CLK1A	AdvancedTCA bused resource Synch clock group 1, bus A
CLK1B	AdvancedTCA bused resource Synch clock group 1, bus A
CLK2	AdvancedTCA bused resource Synch clock group 2
CLK2A	AdvancedTCA bused resource Synch clock group 2, bus A
CLK2B	AdvancedTCA bused resource Synch clock group 2, bus B
CLK3	AdvancedTCA bused resource Synch clock group 3
CLK3A	AdvancedTCA bused resource Synch clock group 3 , bus A
CLK3B	AdvancedTCA bused resource Synch clock group 3 , bus B
CPLD	Complex Programmable Logic Device
CP-TA	Communications Platforms Trade Association

Acronyms	Descriptions
CRC	Cyclic Redundancy Check
CS1	Components Side 1 as describes in PICMG3.0.
CS2	Components Side 2 as describes in PICMG3.0.
CTCA	Compact Telecom Computing Architecture
CTS	Clear To Send
DDR2	(Same as DDR-II). DDR2 SDRAM or Double-Data-Rate two (2) Synchronous Dynamic Random Access Memory.
DHCP	Dynamic Host Configuration Protocol
DIMM	Dual In-line Memory Module
DIN	Deutsches Institut für Normung. German Institute for Standardization.
DMA	Direct Memory Access
DMI	Desktop Management Interface
DPLL	Digital Phase-Locked Loop
DRAM	Dynamic Random Access Memory
DTC	Data Transfer Controller
DTR	Data Terminal Ready
DTS	Digital Thermal Sensor in IA32 processors.
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
EFI	Extensible Firmware Interface
EFT	Electric Fast Transient
EHCI	Enhanced Host Controller Interface. Specification for Universal Serial Bus specification, revision 2.0.
EIA	Electronic Industries Alliance
EISA	Extended Industry Standard Architecture. Superset of ISA, 32-bit bus architecture.
EIST	(Same as SpeedStep). Enhanced Intel SpeedStep Technology
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMTTM	Turbo mode and enhanced Multi Threaded Thermal Management
ERM	Electromagnetic compatibility and Radio spectrum Matters
ESD	ElectroStatic Discharge
ETH	Same as Ethernet.
ETSI	European Telecommunications Standards Institute
FADT	Fixed ACPI Description Table
FC	Fibre Channel
FC-AL	Fibre Channel-Arbitrated Loop
FI	Fabric Interface. Backplane connectivity defined by the ATCA.
FML	Fast Management Link
FPGA	Field-Programmable Gate Array
FPL	FPGA-to-PLD Link. FPL is a 20 MHz serial link that exchange 32-bit of data in each direction between the FPGA and a companion PLD. Comes from Kontron Canada.
FRBx	Fault-Resilient Booting level [1-3]. A term used to describe system features and algorithms that improve the likelihood of the detection of, and recovery from, processor failures in a multiprocessor system.

Acronyms	Descriptions
FRB2	Fault-Resilient Booting, Level 2.
FRT	Free-Running Timer
FRU	Field Replaceable Unit. Any entity that can be replaced by a user in the field. Not all FRUs are hot swappable.
FTP	File Transfer Protocol
FW	FirmWare
FWH	FirmWare Hub. Boot flash connected to the LPC bus containing BIOS FW.
GARP	Generic Attribute Registration Protocol
Gb	Gigabit
GB	(Same as GByte) GigaByte.
GByte	(Same as GB) GigaByte.
GbE	Gigabit Ethernet
GHz	GigaHertz
GMRP	GARP Multicast Registration Protocol
GND	GrouND
GPCM	General-Purpose Chip select Machine
GPI	General Purpose Input
GPIO	General Purpose Input Output
GPO	General Purpose Output
GRUB	GRand Unified Bootloader
GUID	Globally Unique Identifier
GVRP	GARP VLAN Registration Protocol
HFM	High Frequency Mode. The highest operating speed for the processor.
HMS	Hardware Management System
HPM	PICMG Hardware Platform Management specification family
HPM.1	Hardware Platform Management IPM Controller Firmware Upgrade Specification
HW	HardWare
I2C	Inter Integrated Circuit bus
IICH	Integrated I/O Controller Hub. Sub-part of the MICH chipset.
INT	INTerrupt
IMCH	Integrated Memory Controller Hub. Sub-part of the MICH chipset.
IMVP-6	Intel Mobile Voltage Positioning. The Intel Mobile Voltage Positioning specification for the Intel® Core™ Duo Processor. It is a DC-DC converter module that supplies the required voltage and current to a single processor.
IO	(Same as I/O). Input Output
IOAPIC	(Same as IO-APIC). IO Advanced Programmable Interrupt Controller
IOH	I/O Hub
IO-APIC	(Same as IOAPIC). IO Advanced Programmable Interrupt Controller
IOL	IPMI-Over-LAN
IP	Internet Protocol
IPM	Intelligent Platform Management
IPMB	Intelligent Platform Management Bus
IPMB-0	Intelligent Platform Management Bus Channel 0, the logical aggregation of IPMB-A and IPMB-B.

Acronyms	Descriptions
IPMB-A	Intelligent Platform Management Bus A
IPMB-B	Intelligent Platform Management Bus B
IPMB-L	Intelligent Platform Management Bus Local
IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
IPMIFWU	Intelligent Platform Management Interface FirmWare Update
IPv6	Internet Protocol version 6
IRQ	Interrupt ReQuest
ISA	Industry Standard Architecture. 16-bit (XT) bus architecture.
ISE	Xilinx electronic design automation (EDA) tools for use with its devices.
ISO	International Organization for Standardization
ITU	International Telecommunication Union
ITU-T	ITU Telecommunication standardization sector. ITU is International Telecommunication Union.
JTAG	Joint Test Action Group
KB	KiloByte
KHz	KiloHertz
LAN	Local Area Network
LBA	Logical Block Addressing
LBC	Local Bus Controller (On PowerQuicc III CPU)
LED	Light-Emitting Diode
LFM	Low Frequency Mode. The lowest operating speed for the processor.
LIP	Loop Initialization Primitive. Related to FC arbitrated loop topology (an initial message needed for learning the loop addresses and acquiring one).
LSB	Least Significant Byte
LUN	Logical Unit Number
LV	Low Voltage
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
MAC	Media Access Controller address of a computer networking device.
MB	MegaByte
MC	Management Controller
MCH	Memory Controller Hub
MemBIST	(same as MBIST). Memory Built-In Selft-Test. Chipset feature for out-of-band memory testing and intialization.
MDn	Message Digest algorithm (n=2, 5)
MDI	Medium Dependent Interface. MDI port or uplink port.
MHz	MegaHertz
MMC	Module Management Controller. MMCs are linked to the IPMC.
MMIO	Memory-Mapped IO
MP	MultiProcessor
MPS	MultiProcessor Specification
MRC	Memory Reference Code. Chipset specific code provided by the manufacturer and integrated into the BIOS to test and intialize the system memory.

Acronyms	Descriptions
MSB	Most Significant Byte
MSI	Message Signaled Interrupts
MSR	Model Specific Register inside IA32 processors.
MTBF	Mean Time Between Failures
MTRR	Memory Type Range Register. CPU cache control registers.
NAND	Type of Flash Memory, used for mass storage.
NC	Not Connected
NDA	Non-Disclosure Agreement
NEBS	Network Equipment-Building System
NEDS	Network Equipment Development Standard
NMI	Non-Maskable Interrupt
O&M	(Same as OAM/OA&M). Operations and Maintenance
OAM	(Same as OA&M/O&M). Operations, Administration and Maintenance
OA&M	(Same as OAM/O&M). Operations, Administration and Maintenance
OEM	Original Equipment Manufacturer
OMU	Operations and maintenance Unit
OOS	Out Of Service
OS	Operating System
OSI	Open Source Initiative
PCB	Printed Circuit Board
PCIe	(Same as PCI-E). PCI-Express. Next generation I/O standard
PCI-E	(Same as PCIe). PCI-Express. Next generation I/O standard.
PERR	Parity ERRor. A signal on the PCI bus that indicates a parity error on the bus.
PHY	PHYsical layer. Generic electronics term referring to a special electronic integrated circuit or functional block of a circuit that takes care of encoding and decoding between a pure digital domain (on-off) and a modulation in the analog domain.
PICMG	PCI Industrial Computer Manufacturers Group
PICMG®	PCI Industrial Computer Manufacturers Group
PIR	Product Issue Report
PIU	Plug-In Unit
PLCC	Plastic Leaded Chip Carrier
PLD	Programmable Logic Device
PLL	Phase Lock Loop
PMM	POST Memory Manager
PNE	Platform for Network Equipment. A Carrier Grade Linux (4.0) platform.
POR	Power-On Reset
POST	Power-On Self-Test
PXE	Preboot eXecution Environment
RAM	Random Access Memory
RHEL	Red Hat Enterprise Linux
RMS	Root Mean Square
RoHS	Restriction of the Use of Certain Hazardous Substances

Acronyms	Descriptions
ROM	Read Only Memory. Also refers to option ROM or expansion ROM code used during POST to provide services for specific controllers, such as boot capabilities.
RS-232	(Same as RS232). Recommended Standard 232.
RS232	(Same as RS-232). Recommended Standard 232.
RTC	Real Time Clock
RTM	Rear Transition Module
RTS	Request To Send
S0	ACPI OS System State 0. Indicates fully on operating state.
S5	ACPI OS System State 5. Indicates Soft Off operating state.
SBC	Single Board Computer
SBE	Single Bit Error
SCI	System Control Interrupt
SCL	Serial CLock
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic Random Access Memory
SEC	Single-bit Error Correct
SEEPROM	Serial EEPROM
SEL	System Event Log
SERDES	SERializer/DESerializer. Pair of functional blocks commonly used in high speed communications. These blocks convert data between serial data and parallel interfaces in each direction.
SERIRQ	Serial IRQ
SERR	System ERRor. A signal on the PCI bus that indicates a 'fatal' error on the bus.
SGMII	Serial Gigabit Media Independent Interface. Standard interface used to connect a Gigabit Ethernet MAC-block to a PHY.
ShMC	Shelf Management Controller
SMB	(Same as SMBus/SMBUS). System Management Bus.
SMBIOS	System Management BIOS
SMBUS	(Same as SMB/SMBus). System Management Bus.
SMBus	(Same as SMB/SMBUS). System Management Bus.
SMI	System Management Interrupt
SMM	System Management Mode
SMP	Symmetric MultiProcessing. SMP systems allow any processor to work on any task no matter where the data for that task are located in memory; with proper operating system support, SMP systems can easily move tasks between processors to balance the workload efficiently.
SOL	Serial Over LAN
SONET	Synchronous Optical NETworking
SPD	Serial Presence Detect. A standardized way to automatically access information about a computer memory module.
SPI	Serial Peripheral Interface
SSE2	Streaming SIMD Extension 2. SIMD is "Single Instruction, Multiple Data".
SSE3	Streaming SIMD Extension 3. SIMD is "Single Instruction, Multiple Data".
SSH	Secure SHell. A network protocol that allows data to be exchanged over a secure channel between two computers.
TCLKA	Telecom CLocK A. AMC Clock Interface.

Acronyms	Descriptions
TCLKB	Telecom CLocK B. AMC Clock Interface.
TCLKC	Telecom CLocK C. AMC Clock Interface.
TCLKD	Telecom CLocK D. AMC Clock Interface.
TPM	Trusted Platform Module
TX	Transmit
TXD	Transmit
UART	Universal Asynchronous Receiver Transmitter
UL	Underwriters Laboratories inc
USB	Universal Serial Bus
VLAN	Virtual Local Area Network
WD	WatchDog
WDT	WatchDog Timer
XAUI	X (meaning ten) Attachement Unit Interface. A standard for connecting 10 Gigabit Ethernet (10GbE) ports.
XDP	eXtended Debug Port